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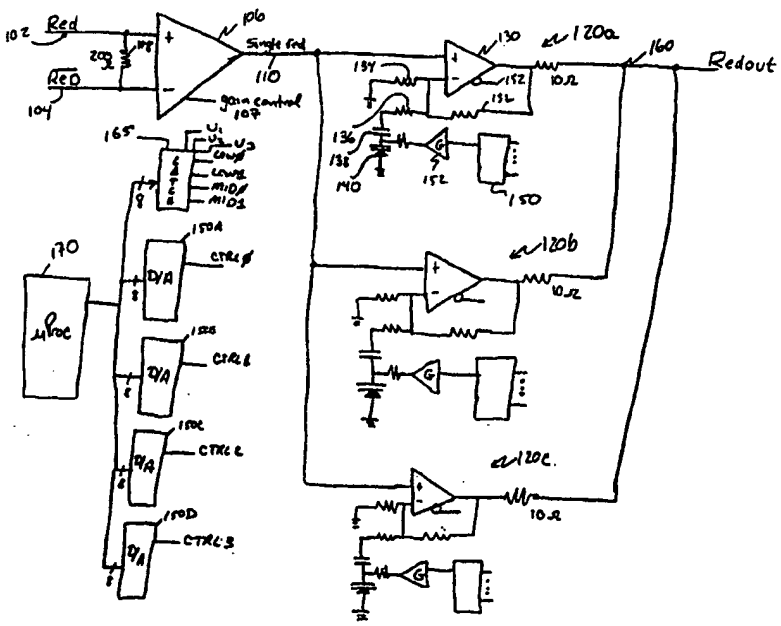

(57) Abstract

An equalization system for compensating the attenuation of high-frequency signals in a twisted wire cable. An equalizing circuit comprises a number of operational amplifiers with a variable impedance connected in a feedback path. The variable impedance comprises a varactor diode whose capacitance changes with the magnitude of a reverse bias voltage. The reverse bias voltage is controlled using a digital-to-analog converter and a gain amplifier to increase the gain of the operational amplifiers at high frequencies. A microprocessor selects the appropriate reverse bias voltages depending on the length of the twisted wire cable to be compensated.

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VIDEO SIGNAL EQUALIZATION SYSTEM

Field of the Invention

The present invention relates to computer systems in general, and in particular to systems for transmitting high-frequency signals over twisted wire cables.

Background of the Invention

In many computer applications, it is desirable to transmit video signals that are created by one computer to a remote location. One example is in a networked computer system whereby one or more server computers that operate the network are located in a dedicated equipment room. Often, these equipment rooms are heavily air-conditioned and are not particularly suited for a human operator that must monitor the operation of the server computers. As a result, there exist systems for controlling the server computers from a remote location so that an operator does not have to be physically present at the server computers. These systems reproduce the video displays created by a server computer and transmit them over a cable to a remote video monitor so that the operator can supervise the operation of the server computers.

Another example of a situation where it is desirable to transmit video signals over some distance is in lecture hall displays. Here it may be desirable to provide several monitors throughout the lecture hall that reproduce the video displays produced by a computer system that is located at the front of the lecture hall.

The most common way of transmitting video signals to a remote location is over a set of twisted wire cables. These cables have the advantage of being relatively inexpensive and are commonly found in many office or factory environments.

One of the problems with twisted wire cables is the loss that occurs at high frequencies. In typical video signals, bandwidths up to 100 MHz are required to transmit high resolution video images. However, at such frequencies, much of the high-frequency components of the video signals transmitted on a twisted wire cable are lost or attenuated. The loss versus frequency for twisted wire cables is generally non-linear and also vary depending upon the length and type of cable used.

While it is possible to replace twisted pair cables with low loss coaxial or fiber-optic cables, such solutions are generally not cost effective. Therefore, there is a need for a system that can compensate for the losses in twisted wire cables so that video or other high-frequency signals may be transmitted over relatively long distances.

Summary of the Invention

To compensate for the high-frequency losses that occur in twisted wire cables, the present invention comprises an equalization network that receives high-frequency signals on a twisted wire cable. A differential amplifier converts a differential signal that is transmitted on a twisted wire cable into a single-ended signal. This single-ended signal is applied to a plurality of equalizing networks, each of which is tunable for a range of cable lengths.

Each equalizing network comprises a non-inverting amplifier and a variable impedance placed in a feedback path of the amplifier. By modifying the impedance, the gain of the amplifier versus frequency can be set to compensate for the losses in the twisted wire cable. The variable impedance preferably comprises a varactor diode that changes capacitance in proportion to a reverse bias DC voltage applied across the diode. A digital-to-analog converter is coupled through a buffer amplifier to the varactor diodes in order to control the reverse bias DC voltage applied to each diode. The digital values written to each of the digital-to-analog converters is controlled by a microprocessor in accordance with the length of twisted wire cable to be compensated.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 illustrates a computer system and a remote workstation that are connected together via a length of twisted wire cable on which high-frequency signals are transmitted;

FIGURE 2 is a block diagram of an equalization network according to the present invention;

FIGURES 3A-3C are more detailed schematic diagrams of the equalization networks according to the present invention; and

FIGURE 4 is a detailed schematic diagram of an alternative embodiment of the equalization network according to the present invention.

Detailed Description of the Preferred Embodiment

As indicated above, the present invention is a system for compensating for high-frequency losses in twisted wire cables. The system is particularly useful for recovering video signals transmitted on twisted wire cables up to 600 feet in length.

FIGURE 1 illustrates a typical environment where it is desirable to transmit video signals on a twisted pair cable. A computer system 10 includes a central processing unit 12, keyboard 14, mouse 16, and video monitor 18. The computer system 10 may be used for a variety of tasks such as controlling a local area network or operating as an Internet gateway, etc. Often, the computer system 10 is located in an environment that is not particularly suited for human operators. For example, the environment may be heavily air-conditioned, or crowded with other computer systems.

In order to avoid having to operate the computer system 10 in its environment, it is often desirable to control the computer system 10 from a remote workstation 30. The workstation 30 generally includes a video monitor 32, keyboard 34, and mouse 36. Commands typed on the keyboard 34 or movements of the mouse 36 operate the remote computer system 10 as if they had been typed on the computer's own keyboard 14, or created by moving the mouse 16. In addition, the video monitor 32 at the workstation displays the same image that is displayed on the video monitor 18 of the remote computer system.

Key strokes entered on the keyboard 34 commands, or movements of the mouse 36 are collected and converted into a format suitable for transmission over a communication link by a signal conditioning unit 40. The keyboard and mouse commands are transmitted over the communication link 42 where they are received by a local signal conditioning unit 44 that converts the keyboard and mouse commands back into their original form and applies them to the computer system 10. Video

signals produced by the computer system 10 are received by the local signal conditioning unit 44 and transmitted over the communication link 42 to the signal conditioning unit 40. The signal conditioning unit 40 conditions the video signals and delivers them to the video monitor 32.

A commercially available system for connecting a workstation to a remote computer is the SWITCHBACK® product available from Apex PC Solutions, Inc., of Woodinville, Washington, the assignee of the present invention. In addition, further descriptions of the signal conditioning units 40 and 44 can be found in U.S. Patent Application Serial No. 08/519,193 or PCT/US96/13772, which are herein incorporated by reference.

As discussed above, the most common type of communication link 42 for connecting remotely located computers are one or more twisted wire cables. These cables are commonly used for Ethernet or token ring-type local area or wide area networks. As discussed above, the problem with twisted wire cables is the signal loss that occurs at high frequencies. For example, in a Category 5 twisted wire cable, a 100 MHz signal is attenuated by a factor of 30 when transmitted over a length of 500 feet. In order to successfully recover video signals transmitted over these types of cables, the signal loss must be recovered. In addition, it is important that the amplitude of the recovered signal remain within +/-1 dB for all its frequency components.

While it may be possible to replace the twisted wire cables with less lossy cables such as large diameter coax or fiber-optic cables, it is often impractical or not cost effective to do so.

FIGURE 2 illustrates a block diagram of an equalization circuit 50 that recovers high-frequency signals that are lost due to the attenuation that occurs in a twisted wire cable. The equalization circuit 50 is located within the signal conditioning unit 40 shown in FIGURE 1 and operates to increase the amplitude of the high-frequency components of video signals that are transmitted from the remote computer system. Although the present invention is described with respect to recovering video signals, those skilled in the art will recognize that the equalization circuit is useful for recovering any high-frequency signal that is transmitted on a twisted wire cable.

As will be appreciated, an RGB color video signal comprises separate red, green, and blue video components. Each of these components is typically transmitted on its own twisted wire cable. In addition, the horizontal and vertical synchronize

signals can be transmitted on separate twisted wire cables or can be mixed in with any of the red, green, or blue video signals as described in U.S. Patent Application Serial No. 08/519,193, referenced above. For purposes of the present application, only the equalization circuit for the red video signal is discussed. However, identical circuits are also provided to equalize the blue and green video signals.

A twisted wire cable generally comprises a first and second copper wire 102, 104 that are twisted around each other. The video signal is transmitted on one of the wires while the inverse of the video signal is transmitted on the other wire. Assuming that the cable and receiving circuitry are properly balanced, the magnetic field created by the video signal is substantially canceled by the inverse video signal transmitted on the other wire in order to reduce cross-talk with neighboring twisted wire cables.

The wire 102 is connected into a non-inverting input of a differential receiver 106 while the wire 104 is coupled to an inverting input of the differential receiver. The differential receiver 106 preferably comprises a CLC 522 amplifier available from National Semiconductor of Denver, Colorado.

A 200 ohm resistor 108 is positioned between the non-inverting and inverting inputs of the differential receiver to control the input impedance of the receiver. The gain of the differential amplifier 106 is nominally set to .615 and can be adjusted by applying a varying voltage to a gain control pin 107. The voltage applied to pin 107 is controlled with an eight-bit digital-to-analog converter (not shown) that produces an output voltage of zero to five volts. The output of the digital-to-analog converter feeds a buffer amplifier having a gain of .396 and a DC offset. The output of the buffer amplifier is connected to the gain control pin 107.

The differential receiver 106 produces a single-ended video signal at its output 110. The single-ended video signal is applied to an input of a number of equalizing networks 120a, 120b, and 120c. Each equalizing network is designed for a range of twisted wire cable lengths. For example, the equalizing network 120a is designed for cable lengths between 300 and 600 feet. The equalizing network 120b is designed for cable lengths between 150 and 250 feet while the equalizing network 120c is designed for cable lengths between zero and 100 feet. In the presently preferred embodiment of the invention, only one of the equalizing networks 120a, 120b, or 120c is activated at a given time.

The equalizing network 120a generally comprises an operational amplifier 130 that is part of a non-inverting gain circuit. The low-frequency gain of the operational amplifier is generally determined by the ratio of a pair of fixed resistors 132 and 134.

The resistor 132 is connected between an output of the amplifier 130 and an inverting input of the amplifier. The fixed resistor 134 is connected between the inverting input of the amplifier 130 and ground.

To compensate for a signal loss that occurs at higher frequencies, a network of variable impedances is also connected between the inverting input of the operational amplifier 130 and ground. The variable impedance comprises a resistor 136 having one terminal coupled to the inverting terminal of the operational amplifier 130. Coupled in series with the resistor 136 is a fixed capacitor 138 and coupled in series between the capacitor 138 and ground is a varactor diode 140. The capacitance of the varactor diode 140 changes with the level of a reverse bias DC voltage that is applied to the diode. The higher the reverse bias voltage, the lower the capacitance. At higher frequencies, the variable impedance defined by the resistor 136, fixed capacitor 138, and varactor diode 140 passes more current, thereby increasing the gain of the operational amplifier 130 to compensate for losses that occur in the twisted wire cable.

To control the reverse bias voltage applied to the varactor diode 140, an eight-bit digital-to-analog converter 150 is provided. A binary value written to the digital-to-analog converter 150 creates a voltage that is increased by an LM342 operation amplifier 152 having a gain of approximately 4. The output of the amplifier 152 is coupled through a resistor to the cathode of the varactor diode 140.

As will be described in further detail below, the particular reverse bias voltage applied to the varactor diode 140 is dependent upon the length of cable that extends between the workstation and the remote computer. To select the particular binary value written to the digital-to-analog converter 150, a microprocessor 170 that is contained within the signal conditioning unit 40 shown in FIGURE 1 writes binary data to a series of digital-to-analog converters 150a, 150b, 150c and 150d. Each of these digital-to-analog converters produces a variable DC voltage on a set of lines, CTRL0, CTRL1, CTRL2 and CTRL3. To set the reverse bias voltages, the microprocessor is programmed to prompt the user for the approximate length of the twisted wire cable currently in use. The user enters the number using the keyboard 34 or highlights an option on the video monitor 32. The microprocessor then uses a look-up table to determine the correct binary value that should be written to the digital-to-analog converters 150a-150d in order to apply the proper reverse bias voltage to the varactor diodes.

As indicated above, one of the equalization circuits 120a, 120b, or 120c is activated depending upon the length of twisted wire cable to be compensated. The activation is performed by placing the appropriate logic signal on an enable pin 152 of the operational amplifier 130. By enabling this pin, the output of the amplifier is taken out of a high impedance state. For a particular cable length, two of the amplifiers associated with the equalization circuits 120a, 120b, or 120c are in a high impedance state while one amplifier is enabled. The output of the amplifiers in each of the equalization circuits are fed through a 10 ohm resistor and joined at a common node 160 where they are fed to a buffer amplifier. The output of the buffer amplifier is sent to the appropriate input of a color monitor.

FIGURE 3A shows in greater detail the equalization circuit 120a that is designed to compensate for attenuation in twisted wire cables having lengths between approximately 300 and 600 feet.

The single-ended video signal produced by the output of the differential amplifier 106, shown in FIGURE 2, is coupled to a non-inverting input of an operational amplifier U_0. A 301 ohm resistor R62 is coupled between an inverting input of the amplifier U_0 and an output of the amplifier. Also disposed between the inverting input of the amplifier U_0 and ground is a 2 K ohm resistor R61. Also coupled to the inverting input of the amplifier U_0 is a variable impedance network that comprises a 10 ohm resistor R41, a 0.01 microfarad capacitor C39 and a BB640 varactor diode D1. The resistor R41 is disposed between the inverting input of the amplifier U_0 and a lead on the capacitor C39. The varactor diode D1 is coupled between another lead of the capacitor C39 and ground.

As described above, a variable reverse bias DC voltage is applied to the cathode of the varactor diode D1. The reverse bias voltage is supplied on the CTRL0 lead from the digital-to-analog converter 150a which is controlled by the microprocessor 170. The output of the digital-to-analog converter 150a is amplified by a buffer amplifier 152 (FIGURE 1). The voltage on the CTRL0 lead is coupled through a 100 K ohm resistor R39 that is connected between the buffer amplifier and the junction of the capacitor C39 and the varactor diode D1.

A second variable impedance comprising a 499 ohm resistor R40, a 56 picofarad capacitor C32 and a BB512 varactor diode D2 is also coupled to the amplifier U_0. One lead of the resistor R40 is coupled to the junction of the resistor R41 and the capacitor C39. The other lead of the resistor R40 is coupled to the capacitor C32. The cathode of the varactor diode D2 is coupled to the other lead

of the capacitor C32, while the anode of the varactor diode D2 is connected to ground. The reverse bias voltage for the varactor diode D2 is supplied on the CTRL1 lead through a 100 K ohm resistor R28 to the junction of the cathode of the varactor diode D2 and the capacitor C32.

The output of amplifier U_0 is coupled through a 49.9 ohm resistor R63 to a non-inverting input of a tri-stateable amplifier U1. Disposed between the output of the amplifier U1 and an inverting input of the amplifier is a 301 ohm resistor R44. Disposed between the non-inverting input of the amplifier U1 and ground is a 4.99 K ohm resistor R43. A variable impedance comprising a 200 ohm resistor R42, a 33 picofarad capacitor C35 and a BB512 varactor diode D4 is also coupled to the inverting input of the amplifier U1. The resistor R42 is coupled between the inverting input of the amplifier and a lead of the capacitor of the C35. The other lead of the capacitor C35 is coupled to the cathode of the varactor diode D4, while the anode of the varactor D4 is grounded. The reverse bias voltage for the diode D4 is supplied on a CTRL2 lead through a 100 K ohm resistor R31 to the junction of capacitor C35 and the cathode of the varactor diode D4.

The equalization circuit 120a also includes another variable impedance comprising a 1 K ohm resistor R30, a 180 picofarad capacitor C34 and a BB512 varactor diode D3. One lead of the resistor R30 is connected to the junction of the resistor R42 and the capacitor C35. Another lead of the resistor R30 is coupled to a lead of the capacitor C34, while the other lead of capacitor C34 is coupled to the cathode of the varactor diode D3. The anode of the varactor diode D3 is grounded. The reverse bias voltage for the varactor diode is supplied on a CTRL3 lead through a 100 K ohm resistor R29 to the junction of the capacitor C34 and the varactor diode D3.

The output of the amplifier U1 is fed through a 10 ohm resistor R45 to the node 160 (shown in FIGURE 2) where it combines with the outputs of the other equalization circuits 120b, and 120c. The tri-stateable amplifier U1 can be placed in a high impedance state by placing the appropriate logic signal on a control lead K1. When this lead is active low, the amplifier U1 is enabled. The particular reverse bias voltages applied to the varactor diodes D1, D2, D3, and D4, in order to compensate for signal losses in cables of 300-600 feet is set forth below.

FIGURE 3B illustrates the equalization circuit 120b used to compensate for attenuation occurring in twisted wire cables having lengths between 150 and 250 feet. The single-ended signal produced by the differential receiver 106 shown in FIGURE 2

is coupled through a 121 ohm resistor R64 to a non-inverting input of a tri-stateable operational amplifier U2. Disposed between an output of the amplifier U2 and an inverting input is a 301 ohm resistor R66. Also coupled between the inverting input of the amplifier U2 and ground is a 4.99 K ohm resistor R71.

To compensate for the signal losses that occur in the cable, a plurality of variable impedances are provided. The first variable impedance comprises a 54.9 ohm resistor R69 that is coupled between the inverting input of the amplifier U2 and a 39 picofarad capacitor C43. The other lead of the capacitor C43 is coupled to a cathode of a BB640 varactor diode D5. An anode of the diode D5 is coupled to a collector terminal of an NPN transistor Q1. A 2 K ohm resistor R50 couples a logic signal MID0 to a base terminal of the transistor. The MID0 signal is set by a latching circuit 165 (FIGURE 2) that is controlled by the microprocessor 170. The reverse bias voltage on the diode D5 is supplied on a CTRL0 line through a 100 K ohm resistor R46 that is coupled to the junction of the capacitor C43 and the cathode of varactor diode D5.

A second variable impedance comprises a 75 ohm resistor R70, a 15 picofarad capacitor C44, a BB639 varactor diode D6, and a transistor Q2. A lead of the resistor R70 is coupled to the junction of the resistor R69 and the capacitor C43. Another lead of the resistor R70 is coupled to a lead of the capacitor C44. A cathode of the varactor diode D6 is coupled to the other lead of the capacitor C44 while the anode of the varactor diode D6 is coupled to the collector terminal of the transistor Q2. A logic signal MID1 is coupled through a 2 K ohm resistor R34 to a base terminal of the transistor Q2. The emitter terminal of the transistor Q2 is grounded. The reverse bias voltage applied to the cathode of diode D6 is also supplied on the CTRL0 line through a 100 K ohm resistor R47 that is connected to the junction of capacitor C44 and the cathode of the varactor diode D6.

A third variable impedance comprises a 100 ohm resistor R72, a 27 picofarad capacitor C45, and a BB640 varactor diode D7. A lead of the resistor R72 is coupled to the junction of resistor R70 and capacitor C44, while another lead of the resistor R72 is coupled to a lead of capacitor C45. A cathode of the varactor diode D7 is coupled to the other lead of the capacitor C45, while the anode of the varactor diode D7 is grounded. The reverse bias voltage provided to the varactor diode D7 supplied on the CTRL1 line through a 100 K ohm resistor R48 that is coupled to the junction of capacitor C45 and the cathode of varactor diode D7.

A fourth variable impedance comprises a 301 ohm resistor R73, a 39 picofarad capacitor C50, and a BB512 varactor diode D8. A lead of the resistor R73 is coupled to the junction of resistor R72 and capacitor C45. Another lead of resistor R73 is coupled to a lead of the capacitor C50. The other lead of capacitor C50 is coupled to the cathode of the varactor diode D8. The reverse bias voltage applied to the varactor diode D8 supplied in the CTRL2 line through a 100 K ohm resistor R49 that is coupled to the junction of the capacitor C50 and the cathode of diode D8.

Finally, a fifth variable impedance comprising a 1.5 K ohm resistor R74, a 100 picofarad capacitor C59, and a BB512 varactor diode D11 is included in the equalization circuit 120b. A lead of the resistor R74 is coupled to the junction of the resistor R73 and the capacitor C50. Another lead of the resistor R74 is coupled to a lead the capacitor C59. The other lead of the capacitor C59 is coupled to the cathode of the varactor diode D11, while the anode of the varactor diode D11 is grounded. The reverse bias voltage applied to the varactor diode D11 is supplied on the CTRL3 line through a 100 K ohm resistor R92 that is coupled to the junction of the capacitor C59 and the cathode of varactor diode D11. The tri-stateable amplifier U2 is set in either its high impedance or active state by applying an appropriate logic signal on a control pin K2.

The magnitude of the reverse bias voltages applied to the varactor diodes D5, D6, D7, D8, and D11 are described in detail below along with the logic signals applied to the base terminals of the transistors Q1 and Q2.

FIGURE 3C shows in greater detail the equalization circuit 120c that is used to recover video signals that are attenuated in twisted wire cables having lengths up to 100 feet. The single-ended video signal produced by the output of the differential receiver 106 shown in FIGURE 2 is applied through a 100 ohm resistor R82 into a non-inverting terminal of a tri-stateable operational amplifier U3. Also coupled between the non-inverting input and ground is a 124 ohm resistor R83. Disposed between an output of the amplifier U3 and an inverting input is a 499 ohm resistor R68. A 332 ohm resistor R85 is coupled between the non-inverting input and ground.

To compensate for losses that occur in the cable, a variable impedance comprising a 130 ohm resistor R84, an 18 picofarad capacitor C55, a BB640 varactor diode D9, and an NPN transistor Q3 are provided. A lead of the resistor R84 is coupled to the inverting input of the amplifier U3, while another lead of the resistor R84 is coupled to a lead of the capacitor C55. The cathode of varactor diode D9 is coupled to the other lead of capacitor C55, while the anode of varactor diode D9 is

coupled to a collector terminal of the transistor Q3. The emitter terminal of transistor Q3 is grounded. The transistor Q3 is activated by a LOW0 logic signal which is applied through a 2 K ohm resistor R75 to a base terminal of the transistor Q3. The reverse bias voltage applied to the varactor diode D9 is supplied on the CTRL0 line through a 100 K ohm resistor R86 that is coupled to the junction of the capacitor C55 and the cathode of the varactor diode D9.

Another variable impedance comprises a 301 ohm resistor R88, a 33 picofarad capacitor C57, and a BB640 varactor diode D16. A lead of the resistor R88 is coupled to the junction of resistor R84 and capacitor C55. Another lead of resistor R88 is coupled to a lead of the capacitor C57. The other lead of capacitor C57 is coupled to the cathode of varactor diode D16. The anode of varactor diode D16 is coupled to a collector terminal of an NPN transistor Q4 while an emitter terminal of the transistor is grounded. The reverse bias voltage applied to the varactor diode D16 is supplied on the CTRL1 line through a 100 K ohm resistor R102 that is coupled to the junction of capacitor C57 and varactor diode D16.

The last variable impedance included in the equalization circuit 120c comprises a 1 K ohm resistor R89, a 120 picofarad capacitor C56, and a BB512 varactor diode D10. A lead of the resistor R89 is coupled to the junction of the resistor R88 and the capacitor C57. Another lead of the resistor R89 is coupled to a lead of the capacitor C56. The cathode of the varactor diode D10 is coupled the other lead of the capacitor C56. The anode of varactor diode D10 is also coupled to the collector terminal of the transistor Q4. The transistor Q4 is driven by the LOW1 logic signal which is applied through a 2 K ohm resistor R35 to a base terminal of the transistor Q4. The equalization circuit 120c is activated by placing an appropriate logic signal on an enable pin K3 of the tri-stateable amplifier U3.

As indicated above, the tri-stateable amplifiers in each equalization circuits 120a, 120b, and 120c are selectively enabled and the varactor diodes of the circuits are supplied with the appropriate reverse bias voltages to compensate for signal losses that occur in the twisted pair lines. The following table defines the reverse bias voltage to be supplied on the CTRL0, CTRL1, CTRL2, and CTRL3 lines for Category 5 twisted wire cables having lengths between 25 and 600 feet. The values listed in the table are set forth in base 16. These values can be converted to absolute voltages produced at the output of the buffer amplifiers by converting the number listed to base 10, and multiplying by approximately 0.0758.

Cable Length Look Up Table (CAT 5) CMC'S INSTALLED

DAC Table (Base 16)

LENGTH OF CABLE	CTRLØ	CTRL1	CTRL2	CTRL3
25	00	00	00	00
50	00	00	00	00
100	40	90	90	20
150	30	90	50	50
200	00	90	50	00
250	00	00	00	00
300	50	50	10	20
350	25	40	40	20
400	20	30	40	10
450	07	10	50	10
500	05	00	50	00
550	05	00	00	00
600	05	00	00	00

The following table describes the logic used to enable the various tri-stateable operational amplifiers in each of the equalization circuits 120a, 120b, and 120c as well as the logic levels to be applied to the transistors in the equalization circuits. A 0 in the table indicates a logic low signal, while a 1 indicates a logic high signal, and an X indicates a don't care condition. These logic levels are set by the latch circuit 165 shown in FIGURE 2, where the U1 line enables the amplifier U1, the U2 line enables the amplifier U2 and the U3 line enables the amplifier U3.

Latch Table

CABLE LENGTH	U_3	U_2	U_1	LOW1	LOW0	MID1	MID0
25	1	0	0	0	1	X	X
50	1	0	0	1	1	X	X
100	0	1	0	X	X	1	0
150	0	1	0	X	X	1	0
200	0	1	0	0	0	1	1
250	0	1	0	0	0	1	1
300	0	0	1	X	X	X	X
350	0	0	1	X	X	X	X
400	0	0	1	X	X	X	X
450	0	0	1	X	X	X	X

FIGURE 4 illustrates an alternative, and currently preferred, equalization network according to the present invention. The equalization network shown in

FIGURE 4 is similar in operation to the equalization networks described above and shown in FIGURES 3A-3C but contains fewer components and can fit on a smaller printed circuit board.

The equalization network comprises a differential receiver 206 that receives a video signal on a twisted wire pair coupled to an inverting and noninverting input of the differential receiver. If need be, a transformer T3 can be placed in line with the video signals on the twisted wire cable to remove any common mode noise signals. A 100 ohm resistor R124 is coupled between the inverting and noninverting input of the differential receiver 206. A pair of 10 K ohm resistors R123 and R125 are coupled from the inverting and noninverting inputs to ground in order to control the input impedance of the differential amplifier. The gain of the differential amplifier is set by a 787 ohm resistor R150 placed between pins 10 and 12, and a 464 ohm resistor R128 placed between pins 4 and 5. In addition, the DC gain of the differential receiver 206 can be adjusted by varying the DC voltage on pin 2.

The single-ended video signal produced at the output of the differential receiver 206 is applied to an operational amplifier U4 that is connected in a noninverting configuration. The single-ended video signal is applied to a noninverting input of the amplifier U4. The DC gain of the amplifier is set by a 301 ohm resistor R173 coupled between an output of the amplifier and the inverting input. Similarly, a 4.99 K ohm resistor R160 is coupled between the inverting input and ground.

To compensate for high frequency losses in the twisted wire cable, the amplifier U4 includes several variable impedances that are connected in the feedback loop of the amplifier. The first variable impedance comprises a 10 ohm resistor R178, a 100 picofarad capacitor C165, a BB512 varactor diode D14, and an NPN transistor Q16. One lead of the resistor R178 is connected to the inverting input of the amplifier U4. The other lead of the resistor R178 is coupled to a lead of the 100 picofarad capacitor C165. The other lead of the capacitor C165 is coupled to the cathode of a BB512 varactor diode D14. The anode of the diode D14 is coupled to a collector terminal of the NPN transistor Q16. The emitter terminal of the transistor Q16 is grounded. Transistor Q16 is turned on by placing the appropriate digital voltage signal on a BOOST0 lead which is coupled to the base terminal of the transistor Q16 through a 2 K ohm resistor R206. A variable reverse bias voltage is supplied on a CTRL10 line through a 100 K ohm resistor R174 connected to the junction of capacitor C165 and the cathode of varactor diode D14.

A second variable impedance comprises a 499 ohm resistor R184, an 82 picofarad capacitor C179, a BB512 varactor diode D21 and an NPN transistor Q22. One lead of the resistor R184 is coupled to the junction of resistor R178 and the capacitor C165. The other lead of the resistor R184 is coupled to a lead of the capacitor C179. The other lead of capacitor C179 is coupled to a cathode of varactor diode D21, while the anode of varactor diode D21 is coupled to the collector terminal of transistor Q22. The emitter terminal of transistor Q22 is grounded. Transistor Q22 is turned on by an appropriate digital logic signal supplied on a BOOST3 lead, that is connected through a 2 K ohm resistor R238 to the base terminal of the transistor Q22. A variable reverse bias voltage is supplied on a CTRL13 line through a 100 K ohm resistor R218 that is coupled to the junction of capacitor C179 and the cathode of varactor diode D21.

A third variable impedance comprises a 1.5 K ohm resistor R205, a 180 picofarad capacitor C189, a BB512 varactor diode D24 and an NPN transistor Q31. A lead of the resistor R205 is coupled to the junction of resistor R184 and capacitor C179. Another lead of resistor R205 is coupled to a lead of the capacitor C189. The other lead of capacitor C189 is coupled to the cathode of varactor diode D24, while the cathode of the varactor diode D24 is coupled to a collector terminal of transistor Q31. The emitter terminal of transistor Q31 is grounded. The transistor Q31 is turned on by supplying a digital logic signal on a BOOST5 line through a 2 K ohm resistor R246 that is coupled to a base terminal of the transistor Q31. A variable reverse bias voltage is supplied to the varactor diode D24 on an LF10 line through a 100 K ohm resistor R231 that is coupled to the junction of capacitor C189 and the anode of varactor diode D24.

For short cables, it is sometimes necessary to desensitize the amplifier U4 to the variable impedance as described above. Therefore, a 301 ohm resistor R157 is coupled between an inverting input of the amplifier U4 and a collector terminal of a transistor Q13. An emitter terminal of transistor Q13 is grounded. The transistor is turned on by a digital logic signal applied on a BOOST6 line through a 2 K ohm resistor R151 that is coupled to a base terminal of the transistor Q13.

The output of the amplifier U4 is coupled through a 49.9 ohm resistor R172 to a noninverting input of an operational amplifier U5. Again, the amplifier is connected in a noninverting configuration with a 301 ohm resistor R193 coupled between an output of the amplifier and an inverting input. Connected between the inverting input and ground is a 4.99 K ohm resistor R204. To compensate for

additional losses in the twisted wire cable, a plurality of variable impedances are also connected in the feedback path of the amplifier. A first variable impedance comprises a 10 ohm resistor R203, a 10 picofarad capacitor C186, a BB640 varactor diode D20 and an NPN transistor Q26. One lead of the resistor R203 is coupled to an inverting input of the amplifier U5. Another lead of the resistor R203 is coupled to a lead of the capacitor C186. The other lead of capacitor C186 is coupled to the cathode of the varactor diode D20, while the anode of diode D20 is coupled to a collector terminal of the transistor Q26. The emitter terminal of transistor Q26 is grounded. A variable reverse bias voltage is supplied on a CTRL11 lead through a 100 K ohm resistor R221 that is coupled to the junction of capacitor C186 and diode D20. The transistor Q26 is turned on by a digital logic signal supplied on a BOOST1 line through a 2 K ohm resistor R245 coupled to a base of the transistor Q26.

A second variable impedance comprises a 200 ohm resistor R212, a 33 picofarad capacitor C194, a BB640 varactor diode D27, and an NPN transistor Q30. One lead of the resistor R212 is coupled to the junction of resistor R203 and capacitor C186. The other lead of resistor R212 is coupled to a lead of the capacitor C194. The other lead of capacitor C194 is coupled to the cathode of diode D27, while the anode of diode D27 is coupled to a collector terminal of the transistor Q30. The emitter terminal of transistor Q30 is grounded. A variable reverse bias voltage is supplied to the diode D27 on a CTRL12 line through a 100 K ohm resistor R229, which is coupled to the junction of the capacitor C194 and diode D27. The transistor Q30 is turned on by a digital logic signal supplied on a BOOST2 line through a 2 K ohm resistor R249 that is coupled to a base terminal of the transistor Q30.

A third variable impedance comprises a 909 ohm resistor R217, a 180 picofarad capacitor C195, a BB512 varactor diode D30 and an NPN transistor Q34. One lead of the resistor R217 is coupled to the junction of resistor R212 and capacitor C194. The other lead of resistor R217 is coupled to a lead of the capacitor C195. The other lead of capacitor C195 is coupled to the cathode of varactor diode D30, while the anode of diode D30 is coupled to a collector terminal of transistor Q34. The emitter terminal of transistor Q34 is grounded. A variable reverse bias voltage is supplied on an LF11 line through a 100 K ohm resistor R230 that is coupled to the junction of capacitor C195 and diode D30. The transistor Q34 is turned on by a digital logic signal applied on a BOOST4 lead through a 2 K ohm resistor R250 coupled to a base terminal of the transistor Q34.

The output of the amplifier U5 is coupled through a 49.9 ohm resistor R171 to a buffer amplifier (not shown). The output of the buffer amplifier is sent to the appropriate input of a color monitor.

The following table defines the reverse bias DC voltages that are applied to the varactor diodes in order to compensate for various lengths of twisted wire cables.

LENGTH OF CABLE	CTRL10	CTRL11	CTRL12	CTRL13	LF10	LF11	DC
25	X	FF	X	X	5C	X	40
50	X	FF	X	X	X	69	40
100	C5	9E	X	X	2E	69	40
150	X	FF	X	5C	48	X	50
200	X	FF	X	6A	48	X	50
250	X	01	X	5C	28	5C	50
300	FF	X	7	69	9F	42	55
350	C0	X	7	52	80	36	55
400	A2	X	7	40	40	30	55
450	60	FF	7	30	25	25	55
500	45	7F	7	27	15	21	60
550	45	5C	7	27	0D	0A	60
600	21	5C	7	27	0D	05	60

The following table describes the logic used to enable the transistors to turn on the varactor diodes in each of the variable impedances to boost the gain of the amplifiers.

LENGTH OF CABLE	BOOST0	BOOST1	BOOST2	BOOST3	BOOST4	BOOST5	BOOST6
25	0	1	0	0	0	1	1
50	0	1	0	0	1	0	1
100	0	1	0	0	0	1	1
150	0	1	0	1	0	1	0
200	0	1	0	1	0	0	0
250	0	1	0	1	1	1	0
300	1	0	1	1	1	1	0
350	1	0	1	1	1	1	0
400	1	0	1	1	1	1	0
450	1	1	1	1	1	1	1
500	1	1	1	1	1	1	1
550	1	1	1	1	1	1	1
600	1	1	1	1	1	1	1

A 0 in the table indicates a logic low signal, while a 1 indicates a logic high signal, and an x indicates a don't care condition. The logic signals are supplied by a latching circuit that is controlled by the microprocessor 170, shown in FIGURE 2.

As will be appreciated, in order to compensate the three colors provided in the video signal, two additional circuits of the type shown in FIGURE 4 are required for the other two video colors.

As can be seen from the above description, the present invention allows high-frequency signals such as video signals to be transmitted on twisted wire cables up to 600 feet in length. However, those skilled in the art will recognize that additional lengths could be accommodated using the same techniques. Because the loss curve of the twisted wire cables does not exhibit a simple slope with respect to frequency, numerous compensation stages must be provided to create a piecewise linear fit. Using the compensation system of the present invention, response curves that are flat to within ± 1 dB up to 100 MHz or more, can be obtained using Category 5 cable up to 600 feet in length.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention. It is therefore intended that the scope of the claims be determined from the following claims and equivalents thereto.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A system for compensating high-frequency signal losses in a twisted wire cable, comprising:

a differential receiver that receives a differential signal on a twisted wire cable;

one or more equalizing networks that receive a signal from an output of the differential receiver, the equalizing networks including a feedback controller amplifier having a variable impedance disposed in a feedback path, the variable impedance including a varactor diode having a capacitance that varies in accordance with a reverse bias voltage applied to the diode, and a circuit that applies a variable reverse bias voltage to the varactor diode in accordance with a length of the twisted wire cable to be compensated.

2. The system of Claim 1, wherein the feedback controlled amplifier comprises an operational amplifier having an inverting and a non-inverting input, and wherein the variable impedance comprises a fixed capacitor disposed between the non-inverting input and the varactor diode.

3. The system of Claim 2, wherein the variable impedance comprises a fixed resistor disposed between the non-inverting input of the operational amplifier and the fixed capacitor.

4. The system of Claim 1, wherein the circuit that applies a variable reverse bias voltage to the varactor diode comprises a digital-to-analog converter.

5. The system of Claim 4, wherein the circuit that applies a variable reverse bias voltage to the varactor diode further comprises a microprocessor that supplies a binary value to the digital-to-analog converter, wherein the binary value is selected in accordance with the length of the twisted wire cable to be compensated.

6. The system of Claim 5, wherein the circuit that applies a variable reverse bias voltage to the varactor diode further comprises a buffer amplifier disposed between the digital-to-analog converter and the varactor diode

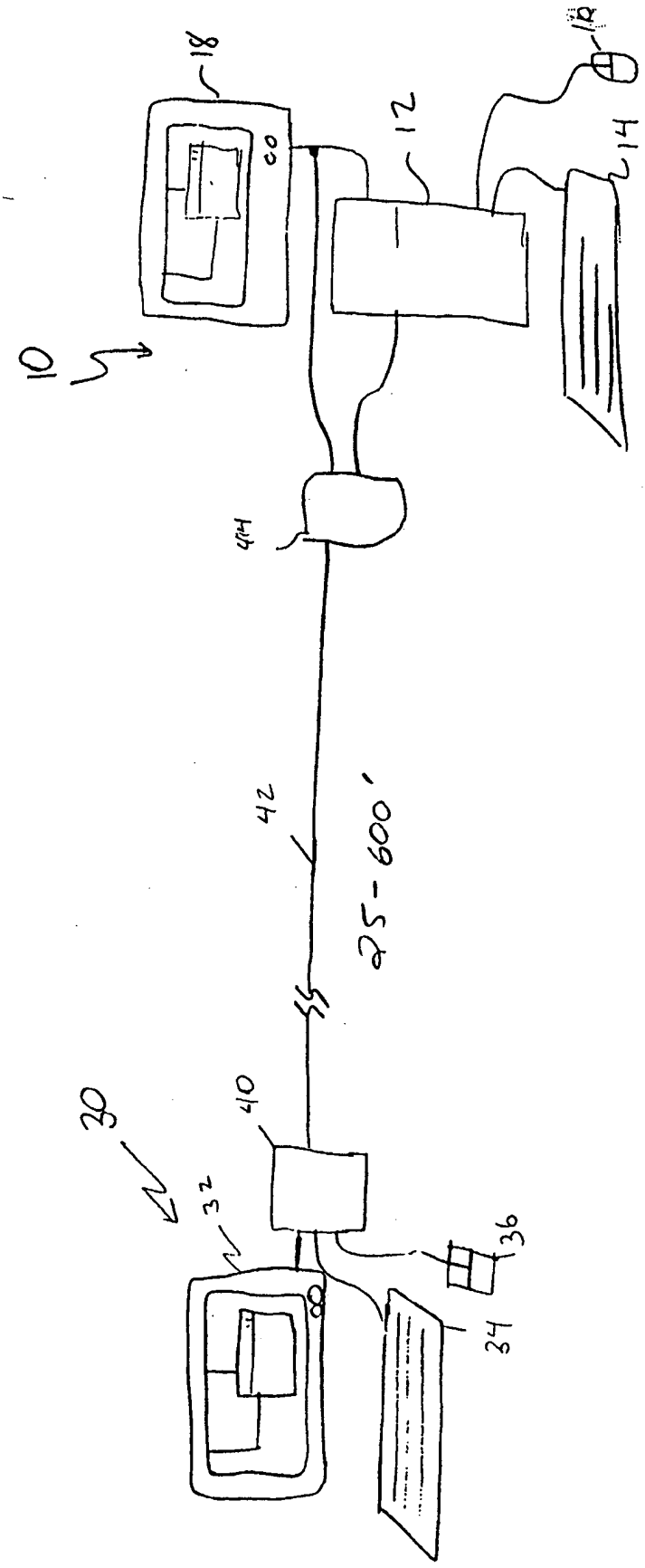

Fig 1

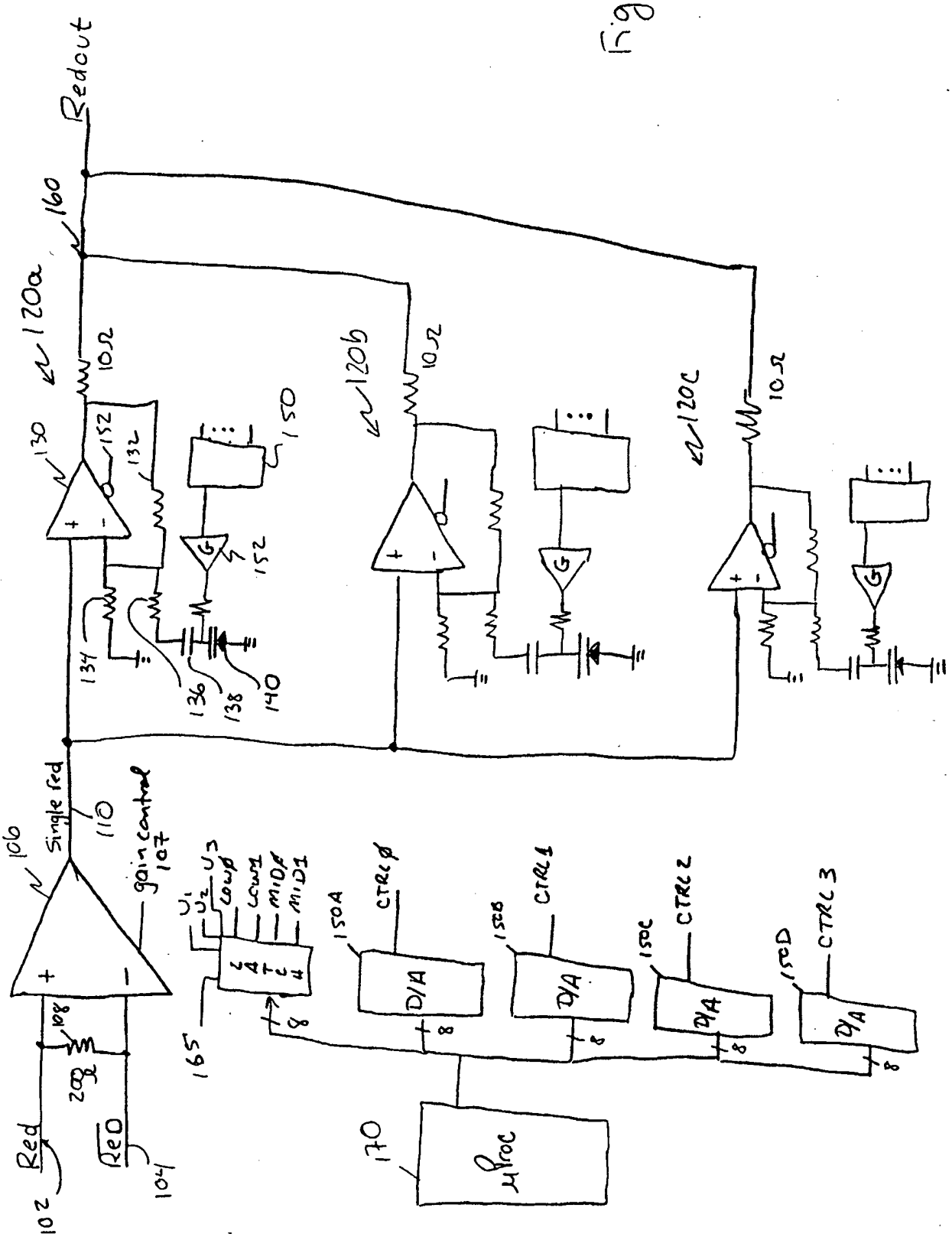
Redout
160
120a
120b
120c
10Ω
130
132
134
136
138
140
150
152
Single red
110
106
gain control
107
Red
102
Red
104
108
200Ω
U1
U2
U3
Comp
Comm
MIDI
MIDI
165
8
150A
150B
150C
150D
CTRL 0
CTRL 1
CTRL 2
CTRL 3
D/A
170
μProc

Fig 2

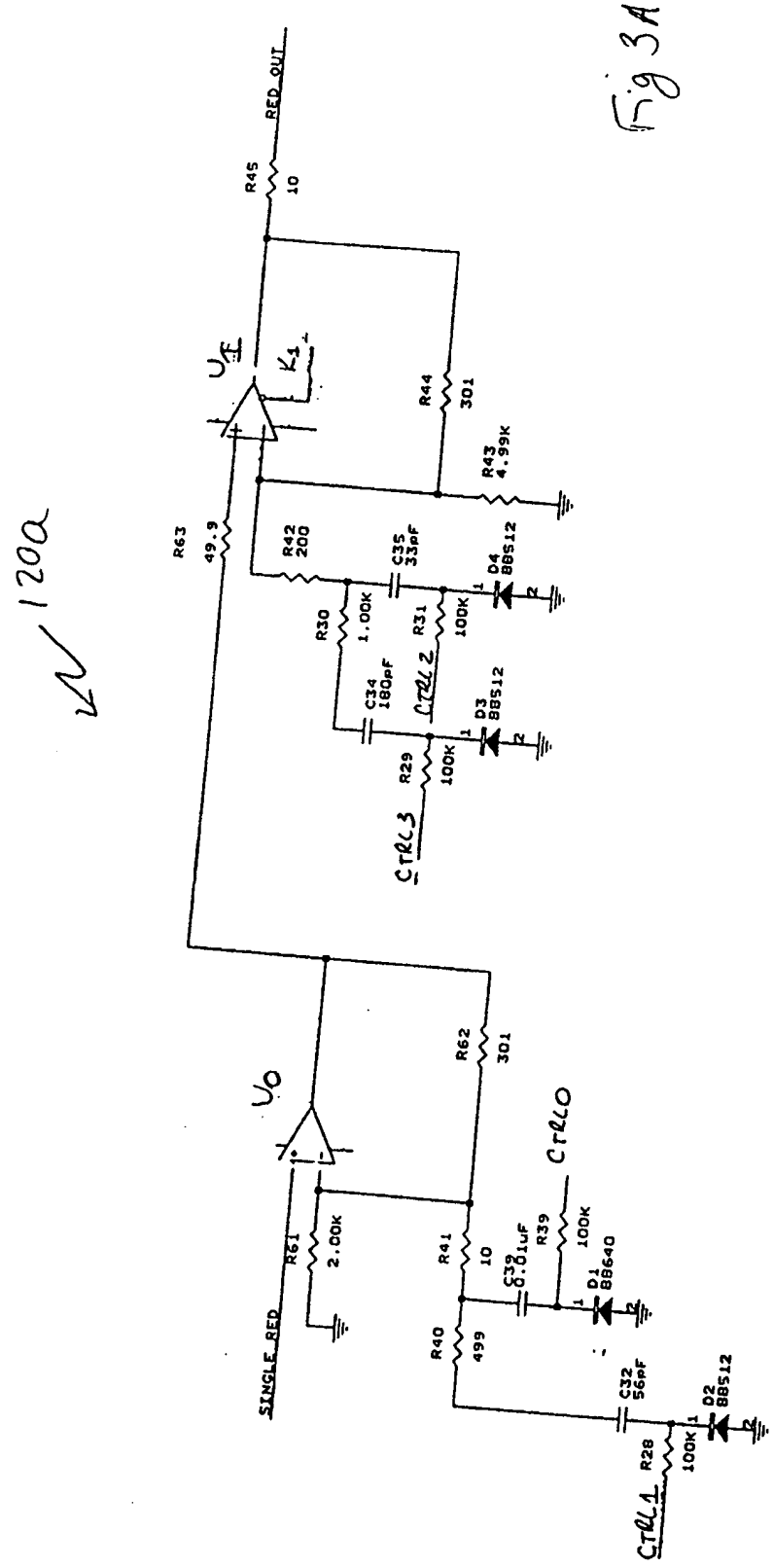
RED OUT
R45
10
R44
301
R43
4.99K
R63
49.9
R42
200
C35
33pF
D4
BBS12
R30
1.00K
R31
100K
C34
180pF
CTRL2
D3
BBS12
R29
100K
CTRL3
R62
301
R61
2.00K
SINGLE RED
R41
10
C39
0.01uF
R39
100K
CTRL0
D1
BB640
R40
499
C32
56pF
D2
BBS12
R28
100K
CTRL1

Fig 3A

120a

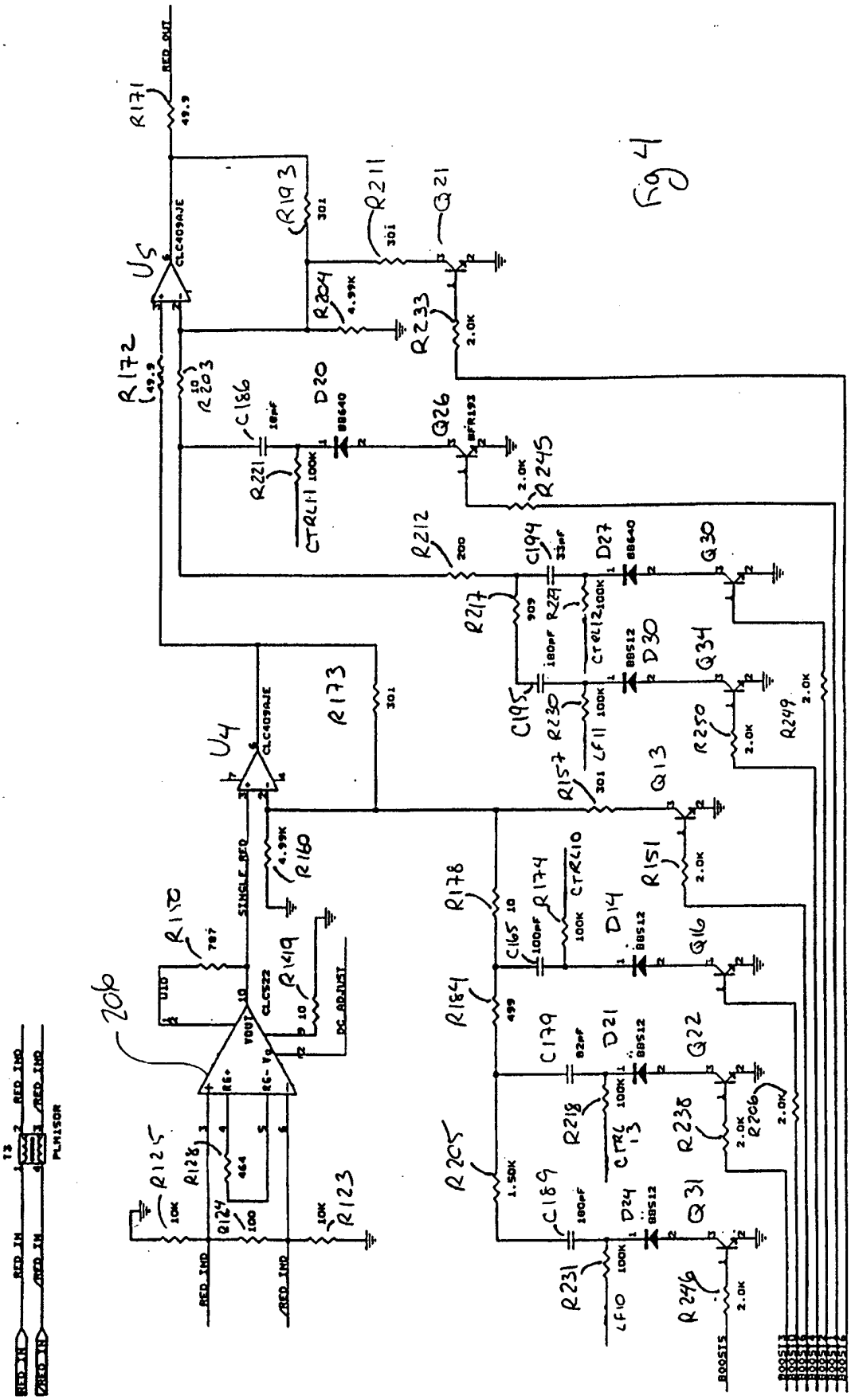
RED OUT
R171
49.9
U5
CLC409AJE
R193
301
R211
301
Q21
R204
4.99K
R233
2.0K
R172
49.9
R203
10
C186
18pF
D20
BB640
Q26
BFR193
R221
100K
CTRL11
R245
2.0K
R212
200
C194
33pF
D27
BB640
Q30
R217
909
R224
100K
CTRL12
C195
180pF
D30
BB512
Q34
R230
100K
CTRL11
R250
2.0K
R249
2.0K
U4
CLC409AJE
R173
301
R157
301
Q13
R151
2.0K
R178
10
C165
100pF
R174
100K
CTRL10
D14
BB512
Q16
R164
499
C179
82pF
D21
BB512
Q22
R218
100K
CTRL13
R238
2.0K
R206
2.0K
R205
1.50K
C189
180pF
D24
BB512
Q31
R231
100K
CTRL10
R246
2.0K
BOOST5
R170
787
SINGLE REQ
4.99K
R160
206
R119
10
DC ADJUST
R125
10K
R126
464
R124
100
R123
10K
RED IND
RED IND
RED IN
RED IN
T3
PLN1508
RED IN
RED IN

Fig 4

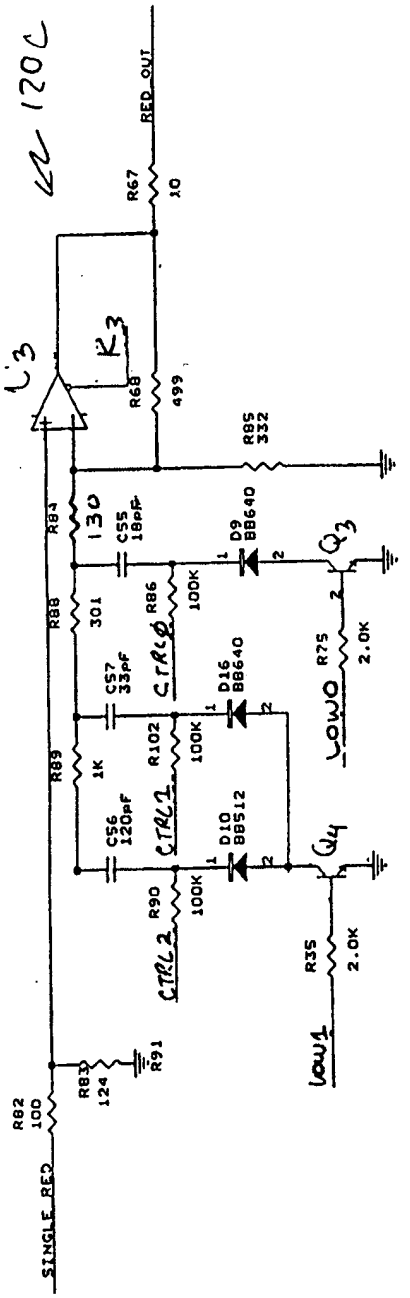
U3
K3
R67
10
RED_OUT
R68
499
R85
332
R84
130
C55
18pF
D9
BB640
Q3
R88
301
C57
33pF
CTRL0
R86
100K
D16
BB640
R89
1K
R102
100K
C56
120pF
CTRL1
D10
BB512
Q4
LOW0
R75
2.0K
R90
100K
CTRL2
R35
2.0K
LOW1
R82
100
R83
124
R91
SINGLE_RED

Fig 3C

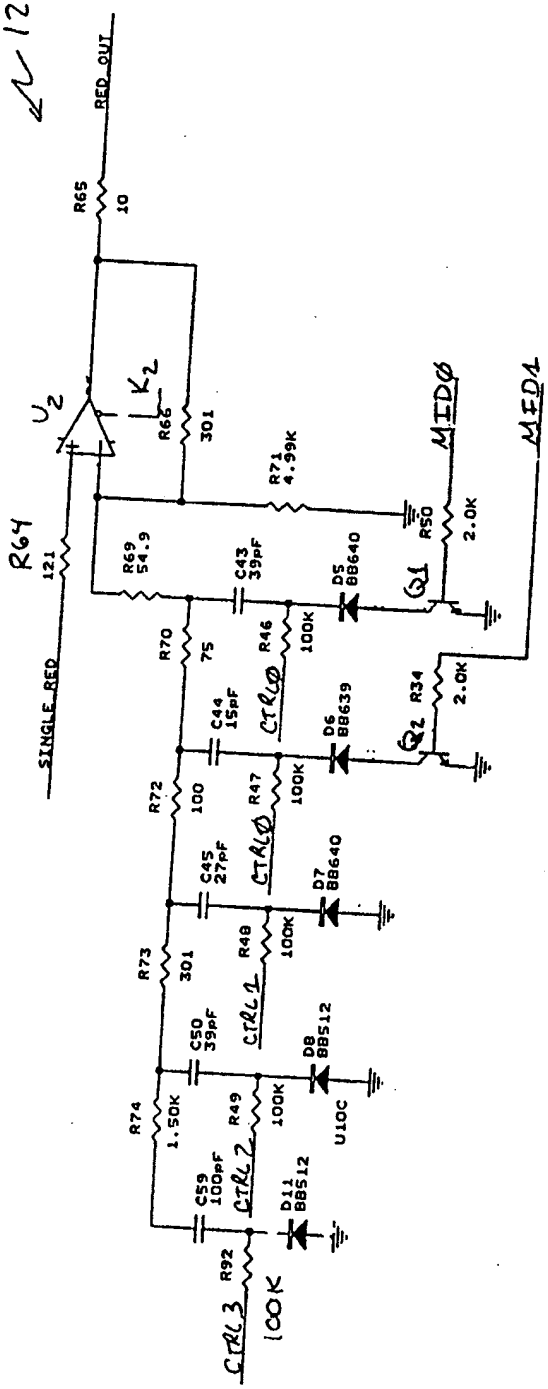
U2
K2
R65
10
RED_OUT
R66
301
R64
121
R71
4.99K
MID0
MED1
R69
54.9
C43
39pF
D5
BB640
Q1
R50
2.0K
SINGLE_RED
R70
75
R46
100K
CTRL0
C44
15pF
D6
BB639
Q2
R34
2.0K
R72
100
R47
100K
CTRL0
C45
27pF
D7
BB640
R73
301
R48
100K
CTRL1
C50
39pF
D8
BB512
U10C
R74
1.50K
R49
100K
CTRL2
C59
100pF
D11
BB512
R92
100K
CTRL3

Fig 3B

VERSION*

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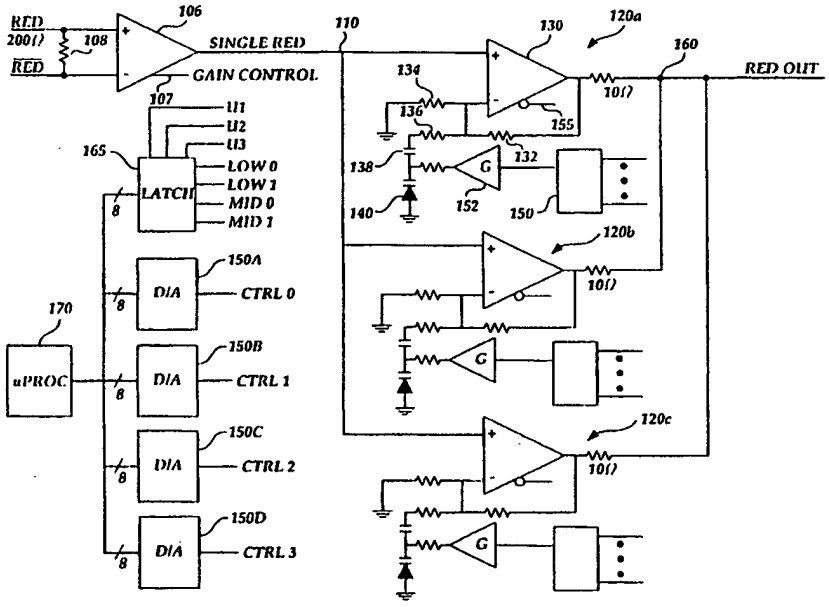

(57) Abstract

An equalization system for compensating the attenuation of high-frequency signals in a twisted wire cable. An equalizing circuit comprises a number of operational amplifiers with a variable impedance connected in a feedback path. The variable impedance comprises a varactor diode whose capacitance changes with the magnitude of a reverse bias voltage. The reverse bias voltage is controlled using a digital-to-analog converter and a gain amplifier to increase the gain of the operational amplifiers at high frequencies. A microprocessor selects the appropriate reverse bias voltages depending on the length of the twisted wire cable to be compensated.

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VIDEO SIGNAL EQUALIZATION SYSTEM

Field of the Invention

The present invention relates to computer systems in general, and in particular to systems for transmitting high-frequency signals over twisted wire cables.

Background of the Invention

In many computer applications, it is desirable to transmit video signals that are created by one computer to a remote location. One example is in a networked computer system whereby one or more server computers that operate the network are located in a dedicated equipment room. Often, these equipment rooms are heavily air-conditioned and are not particularly suited for a human operator that must monitor the operation of the server computers. As a result, there exist systems for controlling the server computers from a remote location so that an operator does not have to be physically present at the server computers. These systems reproduce the video displays created by a server computer and transmit them over a cable to a remote video monitor so that the operator can supervise the operation of the server computers.

Another example of a situation where it is desirable to transmit video signals over some distance is in lecture hall displays. Here it may be desirable to provide several monitors throughout the lecture hall that reproduce the video displays produced by a computer system that is located at the front of the lecture hall.

The most common way of transmitting video signals to a remote location is over a set of twisted wire cables. These cables have the advantage of being relatively inexpensive and are commonly found in many office or factory environments.

One of the problems with twisted wire cables is the loss that occurs at high frequencies. In typical video signals, bandwidths up to 100 MHz are required to transmit high resolution video images. However, at such frequencies, much of the high-frequency components of the video signals transmitted on a twisted wire cable are lost or attenuated. The loss versus frequency for twisted wire cables is generally non-linear and also vary depending upon the length and type of cable used.

While it is possible to replace twisted pair cables with low loss coaxial or fiber-optic cables, such solutions are generally not cost effective. Therefore, there is a need for a system that can compensate for the losses in twisted wire cables so that video or other high-frequency signals may be transmitted over relatively long distances.

Summary of the Invention

To compensate for the high-frequency losses that occur in twisted wire cables, the present invention comprises an equalization network that receives high-frequency signals on a twisted wire cable. A differential amplifier converts a differential signal that is transmitted on a twisted wire cable into a single-ended signal. This single-ended signal is applied to a plurality of equalizing networks, each of which is tunable for a range of cable lengths.

Each equalizing network comprises a non-inverting amplifier and a variable impedance placed in a feedback path of the amplifier. By modifying the impedance, the gain of the amplifier versus frequency can be set to compensate for the losses in the twisted wire cable. The variable impedance preferably comprises a varactor diode that changes capacitance in proportion to a reverse bias DC voltage applied across the diode. A digital-to-analog converter is coupled through a buffer amplifier to the varactor diodes in order to control the reverse bias DC voltage applied to each diode. The digital values written to each of the digital-to-analog converters is controlled by a microprocessor in accordance with the length of twisted wire cable to be compensated.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 illustrates a computer system and a remote workstation that are connected together via a length of twisted wire cable on which high-frequency signals are transmitted;

FIGURE 2 is a block diagram of an equalization network according to the present invention;

FIGURES 3A-3C are more detailed schematic diagrams of the equalization networks according to the present invention; and

FIGURE 4 is a detailed schematic diagram of an alternative embodiment of the equalization network according to the present invention.

Detailed Description of the Preferred Embodiment

As indicated above, the present invention is a system for compensating for high-frequency losses in twisted wire cables. The system is particularly useful for recovering video signals transmitted on twisted wire cables up to 600 feet in length.

FIGURE 1 illustrates a typical environment where it is desirable to transmit video signals on a twisted pair cable. A computer system 10 includes a central processing unit 12, keyboard 14, mouse 16, and video monitor 18. The computer system 10 may be used for a variety of tasks such as controlling a local area network or operating as an Internet gateway, etc. Often, the computer system 10 is located in an environment that is not particularly suited for human operators. For example, the environment may be heavily air-conditioned, or crowded with other computer systems.

In order to avoid having to operate the computer system 10 in its environment, it is often desirable to control the computer system 10 from a remote workstation 30. The workstation 30 generally includes a video monitor 32, keyboard 34, and mouse 36. Commands typed on the keyboard 34 or movements of the mouse 36 operate the remote computer system 10 as if they had been typed on the computer's own keyboard 14, or created by moving the mouse 16. In addition, the video monitor 32 at the workstation displays the same image that is displayed on the video monitor 18 of the remote computer system.

Key strokes entered on the keyboard 34 commands, or movements of the mouse 36 are collected and converted into a format suitable for transmission over a communication link by a signal conditioning unit 40. The keyboard and mouse commands are transmitted over the communication link 42 where they are received by a local signal conditioning unit 44 that converts the keyboard and mouse commands back into their original form and applies them to the computer system 10. Video

signals produced by the computer system 10 are received by the local signal conditioning unit 44 and transmitted over the communication link 42 to the signal conditioning unit 40. The signal conditioning unit 40 conditions the video signals and delivers them to the video monitor 32.

A commercially available system for connecting a workstation to a remote computer is the SWITCHBACK® product available from Apex PC Solutions, Inc., of Woodinville, Washington, the assignee of the present invention. In addition, further descriptions of the signal conditioning units 40 and 44 can be found in U.S. Patent Application Serial No. 08/519,193 or PCT/US96/13772, which are herein incorporated by reference.

As discussed above, the most common type of communication link 42 for connecting remotely located computers are one or more twisted wire cables. These cables are commonly used for Ethernet or token ring-type local area or wide area networks. As discussed above, the problem with twisted wire cables is the signal loss that occurs at high frequencies. For example, in a Category 5 twisted wire cable, a 100 MHz signal is attenuated by a factor of 30 when transmitted over a length of 500 feet. In order to successfully recover video signals transmitted over these types of cables, the signal loss must be recovered. In addition, it is important that the amplitude of the recovered signal remain within +/-1 dB for all its frequency components.

While it may be possible to replace the twisted wire cables with less lossy cables such as large diameter coax or fiber-optic cables, it is often impractical or not cost effective to do so.

FIGURE 2 illustrates a block diagram of an equalization circuit 50 that recovers high-frequency signals that are lost due to the attenuation that occurs in a twisted wire cable. The equalization circuit 50 is located within the signal conditioning unit 40 shown in FIGURE 1 and operates to increase the amplitude of the high-frequency components of video signals that are transmitted from the remote computer system. Although the present invention is described with respect to recovering video signals, those skilled in the art will recognize that the equalization circuit is useful for recovering any high-frequency signal that is transmitted on a twisted wire cable.

As will be appreciated, an RGB color video signal comprises separate red, green, and blue video components. Each of these components is typically transmitted on its own twisted wire cable. In addition, the horizontal and vertical synchronize

signals can be transmitted on separate twisted wire cables or can be mixed in with any of the red, green, or blue video signals as described in U.S. Patent Application Serial No. 08/519,193, referenced above. For purposes of the present application, only the equalization circuit for the red video signal is discussed. However, identical circuits are also provided to equalize the blue and green video signals.

A twisted wire cable generally comprises a first and second copper wire 102, 104 that are twisted around each other. The video signal is transmitted on one of the wires while the inverse of the video signal is transmitted on the other wire. Assuming that the cable and receiving circuitry are properly balanced, the magnetic field created by the video signal is substantially canceled by the inverse video signal transmitted on the other wire in order to reduce cross-talk with neighboring twisted wire cables.

The wire 102 is connected into a non-inverting input of a differential receiver 106 while the wire 104 is coupled to an inverting input of the differential receiver. The differential receiver 106 preferably comprises a CLC 522 amplifier available from National Semiconductor of Denver, Colorado.

A 200 ohm resistor 108 is positioned between the non-inverting and inverting inputs of the differential receiver to control the input impedance of the receiver. The gain of the differential amplifier 106 is nominally set to .615 and can be adjusted by applying a varying voltage to a gain control pin 107. The voltage applied to pin 107 is controlled with an eight-bit digital-to-analog converter (not shown) that produces an output voltage of zero to five volts. The output of the digital-to-analog converter feeds a buffer amplifier having a gain of .396 and a DC offset. The output of the buffer amplifier is connected to the gain control pin 107.

The differential receiver 106 produces a single-ended video signal at its output 110. The single-ended video signal is applied to an input of a number of equalizing networks 120a, 120b, and 120c. Each equalizing network is designed for a range of twisted wire cable lengths. For example, the equalizing network 120a is designed for cable lengths between 300 and 600 feet. The equalizing network 120b is designed for cable lengths between 150 and 250 feet while the equalizing network 120c is designed for cable lengths between zero and 100 feet. In the presently preferred embodiment of the invention, only one of the equalizing networks 120a, 120b, or 120c is activated at a given time.

The equalizing network 120a generally comprises an operational amplifier 130 that is part of a non-inverting gain circuit. The low-frequency gain of the operational amplifier is generally determined by the ratio of a pair of fixed resistors 132 and 134.

The resistor 132 is connected between an output of the amplifier 130 and an inverting input of the amplifier. The fixed resistor 134 is connected between the inverting input of the amplifier 130 and ground.

To compensate for a signal loss that occurs at higher frequencies, a network of variable impedances is also connected between the inverting input of the operational amplifier 130 and ground. The variable impedance comprises a resistor 136 having one terminal coupled to the inverting terminal of the operational amplifier 130. Coupled in series with the resistor 136 is a fixed capacitor 138 and coupled in series between the capacitor 138 and ground is a varactor diode 140. The capacitance of the varactor diode 140 changes with the level of a reverse bias DC voltage that is applied to the diode. The higher the reverse bias voltage, the lower the capacitance. At higher frequencies, the variable impedance defined by the resistor 136, fixed capacitor 138, and varactor diode 140 passes more current, thereby increasing the gain of the operational amplifier 130 to compensate for losses that occur in the twisted wire cable.

To control the reverse bias voltage applied to the varactor diode 140, an eight-bit digital-to-analog converter 150 is provided. A binary value written to the digital-to-analog converter 150 creates a voltage that is increased by an LM342 operation amplifier 152 having a gain of approximately 4. The output of the amplifier 152 is coupled through a resistor to the cathode of the varactor diode 140.

As will be described in further detail below, the particular reverse bias voltage applied to the varactor diode 140 is dependent upon the length of cable that extends between the workstation and the remote computer. To select the particular binary value written to the digital-to-analog converter 150, a microprocessor 170 that is contained within the signal conditioning unit 40 shown in FIGURE 1 writes binary data to a series of digital-to-analog converters 150a, 150b, 150c and 150d. Each of these digital-to-analog converters produces a variable DC voltage on a set of lines, CTRL0, CTRL1, CTRL2 and CTRL3. To set the reverse bias voltages, the microprocessor is programmed to prompt the user for the approximate length of the twisted wire cable currently in use. The user enters the number using the keyboard 34 or highlights an option on the video monitor 32. The microprocessor then uses a look-up table to determine the correct binary value that should be written to the digital-to-analog converters 150a-150d in order to apply the proper reverse bias voltage to the varactor diodes.

As indicated above, one of the equalization circuits 120a, 120b, or 120c is activated depending upon the length of twisted wire cable to be compensated. The activation is performed by placing the appropriate logic signal on an enable pin 152 of the operational amplifier 130. By enabling this pin, the output of the amplifier is taken out of a high impedance state. For a particular cable length, two of the amplifiers associated with the equalization circuits 120a, 120b, or 120c are in a high impedance state while one amplifier is enabled. The output of the amplifiers in each of the equalization circuits are fed through a 10 ohm resistor and joined at a common node 160 where they are fed to a buffer amplifier. The output of the buffer amplifier is sent to the appropriate input of a color monitor.

FIGURE 3A shows in greater detail the equalization circuit 120a that is designed to compensate for attenuation in twisted wire cables having lengths between approximately 300 and 600 feet.

The single-ended video signal produced by the output of the differential amplifier 106, shown in FIGURE 2, is coupled to a non-inverting input of an operational amplifier U_0. A 301 ohm resistor R62 is coupled between an inverting input of the amplifier U_0 and an output of the amplifier. Also disposed between the inverting input of the amplifier U_0 and ground is a 2 K ohm resistor R61. Also coupled to the inverting input of the amplifier U_0 is a variable impedance network that comprises a 10 ohm resistor R41, a 0.01 microfarad capacitor C39 and a BB640 varactor diode D1. The resistor R41 is disposed between the inverting input of the amplifier U_0 and a lead on the capacitor C39. The varactor diode D1 is coupled between another lead of the capacitor C39 and ground.

As described above, a variable reverse bias DC voltage is applied to the cathode of the varactor diode D1. The reverse bias voltage is supplied on the CTRL0 lead from the digital-to-analog converter 150a which is controlled by the microprocessor 170. The output of the digital-to-analog converter 150a is amplified by a buffer amplifier 152 (FIGURE 1). The voltage on the CTRL0 lead is coupled through a 100 K ohm resistor R39 that is connected between the buffer amplifier and the junction of the capacitor C39 and the varactor diode D1.

A second variable impedance comprising a 499 ohm resistor R40, a 56 picofarad capacitor C32 and a BB512 varactor diode D2 is also coupled to the amplifier U_0. One lead of the resistor R40 is coupled to the junction of the resistor R41 and the capacitor C39. The other lead of the resistor R40 is coupled to the capacitor C32. The cathode of the varactor diode D2 is coupled to the other lead

of the capacitor C32, while the anode of the varactor diode D2 is connected to ground. The reverse bias voltage for the varactor diode D2 is supplied on the CTRL1 lead through a 100 K ohm resistor R28 to the junction of the cathode of the varactor diode D2 and the capacitor C32.

The output of amplifier U_0 is coupled through a 49.9 ohm resistor R63 to a non-inverting input of a tri-stateable amplifier U1. Disposed between the output of the amplifier U1 and an inverting input of the amplifier is a 301 ohm resistor R44. Disposed between the non-inverting input of the amplifier U1 and ground is a 4.99 K ohm resistor R43. A variable impedance comprising a 200 ohm resistor R42, a 33 picofarad capacitor C35 and a BB512 varactor diode D4 is also coupled to the inverting input of the amplifier U1. The resistor R42 is coupled between the inverting input of the amplifier and a lead of the capacitor of the C35. The other lead of the capacitor C35 is coupled to the cathode of the varactor diode D4, while the anode of the varactor D4 is grounded. The reverse bias voltage for the diode D4 is supplied on a CTRL2 lead through a 100 K ohm resistor R31 to the junction of capacitor C35 and the cathode of the varactor diode D4.

The equalization circuit 120a also includes another variable impedance comprising a 1 K ohm resistor R30, a 180 picofarad capacitor C34 and a BB512 varactor diode D3. One lead of the resistor R30 is connected to the junction of the resistor R42 and the capacitor C35. Another lead of the resistor R30 is coupled to a lead of the capacitor C34, while the other lead of capacitor C34 is coupled to the cathode of the varactor diode D3. The anode of the varactor diode D3 is grounded. The reverse bias voltage for the varactor diode is supplied on a CTRL3 lead through a 100 K ohm resistor R29 to the junction of the capacitor C34 and the varactor diode D3.

The output of the amplifier U1 is fed through a 10 ohm resistor R45 to the node 160 (shown in FIGURE 2) where it combines with the outputs of the other equalization circuits 120b, and 120c. The tri-stateable amplifier U1 can be placed in a high impedance state by placing the appropriate logic signal on a control lead K1. When this lead is active low, the amplifier U1 is enabled. The particular reverse bias voltages applied to the varactor diodes D1, D2, D3, and D4, in order to compensate for signal losses in cables of 300-600 feet is set forth below.

FIGURE 3B illustrates the equalization circuit 120b used to compensate for attenuation occurring in twisted wire cables having lengths between 150 and 250 feet. The single-ended signal produced by the differential receiver 106 shown in FIGURE 2

is coupled through a 121 ohm resistor R64 to a non-inverting input of a tri-stateable operational amplifier U2. Disposed between an output of the amplifier U2 and an inverting input is a 301 ohm resistor R66. Also coupled between the inverting input of the amplifier U2 and ground is a 4.99 K ohm resistor R71.

To compensate for the signal losses that occur in the cable, a plurality of variable impedances are provided. The first variable impedance comprises a 54.9 ohm resistor R69 that is coupled between the inverting input of the amplifier U2 and a 39 picofarad capacitor C43. The other lead of the capacitor C43 is coupled to a cathode of a BB640 varactor diode D5. An anode of the diode D5 is coupled to a collector terminal of an NPN transistor Q1. A 2 K ohm resistor R50 couples a logic signal MID0 to a base terminal of the transistor. The MID0 signal is set by a latching circuit 165 (FIGURE 2) that is controlled by the microprocessor 170. The reverse bias voltage on the diode D5 is supplied on a CTRL0 line through a 100 K ohm resistor R46 that is coupled to the junction of the capacitor C43 and the cathode of varactor diode D5.

A second variable impedance comprises a 75 ohm resistor R70, a 15 picofarad capacitor C44, a BB639 varactor diode D6, and a transistor Q2. A lead of the resistor R70 is coupled to the junction of the resistor R69 and the capacitor C43. Another lead of the resistor R70 is coupled to a lead of the capacitor C44. A cathode of the varactor diode D6 is coupled to the other lead of the capacitor C44 while the anode of the varactor diode D6 is coupled to the collector terminal of the transistor Q2. A logic signal MID1 is coupled through a 2 K ohm resistor R34 to a base terminal of the transistor Q2. The emitter terminal of the transistor Q2 is grounded. The reverse bias voltage applied to the cathode of diode D6 is also supplied on the CTRL0 line through a 100 K ohm resistor R47 that is connected to the junction of capacitor C44 and the cathode of the varactor diode D6.

A third variable impedance comprises a 100 ohm resistor R72, a 27 picofarad capacitor C45, and a BB640 varactor diode D7. A lead of the resistor R72 is coupled to the junction of resistor R70 and capacitor C44, while another lead of the resistor R72 is coupled to a lead of capacitor C45. A cathode of the varactor diode D7 is coupled to the other lead of the capacitor C45, while the anode of the varactor diode D7 is grounded. The reverse bias voltage provided to the varactor diode D7 supplied on the CTRL1 line through a 100 K ohm resistor R48 that is coupled to the junction of capacitor C45 and the cathode of varactor diode D7.

A fourth variable impedance comprises a 301 ohm resistor R73, a 39 picofarad capacitor C50, and a BB512 varactor diode D8. A lead of the resistor R73 is coupled to the junction of resistor R72 and capacitor C45. Another lead of resistor R73 is coupled to a lead of the capacitor C50. The other lead of capacitor C50 is coupled to the cathode of the varactor diode D8. The reverse bias voltage applied to the varactor diode D8 supplied in the CTRL2 line through a 100 K ohm resistor R49 that is coupled to the junction of the capacitor C50 and the cathode of diode D8.

Finally, a fifth variable impedance comprising a 1.5 K ohm resistor R74, a 100 picofarad capacitor C59, and a BB512 varactor diode D11 is included in the equalization circuit 120b. A lead of the resistor R74 is coupled to the junction of the resistor R73 and the capacitor C50. Another lead of the resistor R74 is coupled to a lead the capacitor C59. The other lead of the capacitor C59 is coupled to the cathode of the varactor diode D11, while the anode of the varactor diode D11 is grounded. The reverse bias voltage applied to the varactor diode D11 is supplied on the CTRL3 line through a 100 K ohm resistor R92 that is coupled to the junction of the capacitor C59 and the cathode of varactor diode D11. The tri-stateable amplifier U2 is set in either its high impedance or active state by applying an appropriate logic signal on a control pin K2.

The magnitude of the reverse bias voltages applied to the varactor diodes D5, D6, D7, D8, and D11 are described in detail below along with the logic signals applied to the base terminals of the transistors Q1 and Q2.

FIGURE 3C shows in greater detail the equalization circuit 120c that is used to recover video signals that are attenuated in twisted wire cables having lengths up to 100 feet. The single-ended video signal produced by the output of the differential receiver 106 shown in FIGURE 2 is applied through a 100 ohm resistor R82 into a non-inverting terminal of a tri-stateable operational amplifier U3. Also coupled between the non-inverting input and ground is a 124 ohm resistor R83. Disposed between an output of the amplifier U3 and an inverting input is a 499 ohm resistor R68. A 332 ohm resistor R85 is coupled between the non-inverting input and ground.

To compensate for losses that occur in the cable, a variable impedance comprising a 130 ohm resistor R84, an 18 picofarad capacitor C55, a BB640 varactor diode D9, and an NPN transistor Q3 are provided. A lead of the resistor R84 is coupled to the inverting input of the amplifier U3, while another lead of the resistor R84 is coupled to a lead of the capacitor C55. The cathode of varactor diode D9 is coupled to the other lead of capacitor C55, while the anode of varactor diode D9 is

coupled to a collector terminal of the transistor Q3. The emitter terminal of transistor Q3 is grounded. The transistor Q3 is activated by a LOW0 logic signal which is applied through a 2 K ohm resistor R75 to a base terminal of the transistor Q3. The reverse bias voltage applied to the varactor diode D9 is supplied on the CTRL0 line through a 100 K ohm resistor R86 that is coupled to the junction of the capacitor C55 and the cathode of the varactor diode D9.

Another variable impedance comprises a 301 ohm resistor R88, a 33 picofarad capacitor C57, and a BB640 varactor diode D16. A lead of the resistor R88 is coupled to the junction of resistor R84 and capacitor C55. Another lead of resistor R88 is coupled to a lead of the capacitor C57. The other lead of capacitor C57 is coupled to the cathode of varactor diode D16. The anode of varactor diode D16 is coupled to a collector terminal of an NPN transistor Q4 while an emitter terminal of the transistor is grounded. The reverse bias voltage applied to the varactor diode D16 is supplied on the CTRL1 line through a 100 K ohm resistor R102 that is coupled to the junction of capacitor C57 and varactor diode D16.

The last variable impedance included in the equalization circuit 120c comprises a 1 K ohm resistor R89, a 120 picofarad capacitor C56, and a BB512 varactor diode D10. A lead of the resistor R89 is coupled to the junction of the resistor R88 and the capacitor C57. Another lead of the resistor R89 is coupled to a lead of the capacitor C56. The cathode of the varactor diode D10 is coupled the other lead of the capacitor C56. The anode of varactor diode D10 is also coupled to the collector terminal of the transistor Q4. The transistor Q4 is driven by the LOW1 logic signal which is applied through a 2 K ohm resistor R35 to a base terminal of the transistor Q4. The equalization circuit 120c is activated by placing an appropriate logic signal on an enable pin K3 of the tri-stateable amplifier U3.

As indicated above, the tri-stateable amplifiers in each equalization circuits 120a, 120b, and 120c are selectively enabled and the varactor diodes of the circuits are supplied with the appropriate reverse bias voltages to compensate for signal losses that occur in the twisted pair lines. The following table defines the reverse bias voltage to be supplied on the CTRL0, CTRL1, CTRL2, and CTRL3 lines for Category 5 twisted wire cables having lengths between 25 and 600 feet. The values listed in the table are set forth in base 16. These values can be converted to absolute voltages produced at the output of the buffer amplifiers by converting the number listed to base 10, and multiplying by approximately 0.0758.

Cable Length Look Up Table (CAT 5) CMC'S INSTALLED

DAC Table (Base 16)

LENGTH OF CABLE	CTRLØ	CTRL1	CTRL2	CTRL3
25	00	00	00	00
50	00	00	00	00
100	40	90	90	20
150	30	90	50	50
200	00	90	50	00
250	00	00	00	00
300	50	50	10	20
350	25	40	40	20
400	20	30	40	10
450	07	10	50	10
500	05	00	50	00
550	05	00	00	00
600	05	00	00	00

The following table describes the logic used to enable the various tri-stateable operational amplifiers in each of the equalization circuits 120a, 120b, and 120c as well as the logic levels to be applied to the transistors in the equalization circuits. A 0 in the table indicates a logic low signal, while a 1 indicates a logic high signal, and an X indicates a don't care condition. These logic levels are set by the latch circuit 165 shown in FIGURE 2, where the U1 line enables the amplifier U1, the U2 line enables the amplifier U2 and the U3 line enables the amplifier U3.

Latch Table

CABLE LENGTH	U_3	U_2	U_1	LOW1	LOW0	MID1	MID0
25	1	0	0	0	1	X	X
50	1	0	0	1	1	X	X
100	0	1	0	X	X	1	0
150	0	1	0	X	X	1	0
200	0	1	0	0	0	1	1
250	0	1	0	0	0	1	1
300	0	0	1	X	X	X	X
350	0	0	1	X	X	X	X
400	0	0	1	X	X	X	X
450	0	0	1	X	X	X	X

FIGURE 4 illustrates an alternative, and currently preferred, equalization network according to the present invention. The equalization network shown in

FIGURE 4 is similar in operation to the equalization networks described above and shown in FIGURES 3A-3C but contains fewer components and can fit on a smaller printed circuit board.

The equalization network comprises a differential receiver 206 that receives a video signal on a twisted wire pair coupled to an inverting and noninverting input of the differential receiver. If need be, a transformer T3 can be placed in line with the video signals on the twisted wire cable to remove any common mode noise signals. A 100 ohm resistor R124 is coupled between the inverting and noninverting input of the differential receiver 206. A pair of 10 K ohm resistors R123 and R125 are coupled from the inverting and noninverting inputs to ground in order to control the input impedance of the differential amplifier. The gain of the differential amplifier is set by a 787 ohm resistor R150 placed between pins 10 and 12, and a 464 ohm resistor R128 placed between pins 4 and 5. In addition, the DC gain of the differential receiver 206 can be adjusted by varying the DC voltage on pin 2.

The single-ended video signal produced at the output of the differential receiver 206 is applied to an operational amplifier U4 that is connected in a noninverting configuration. The single-ended video signal is applied to a noninverting input of the amplifier U4. The DC gain of the amplifier is set by a 301 ohm resistor R173 coupled between an output of the amplifier and the inverting input. Similarly, a 4.99 K ohm resistor R160 is coupled between the inverting input and ground.

To compensate for high frequency losses in the twisted wire cable, the amplifier U4 includes several variable impedances that are connected in the feedback loop of the amplifier. The first variable impedance comprises a 10 ohm resistor R178, a 100 picofarad capacitor C165, a BB512 varactor diode D14, and an NPN transistor Q16. One lead of the resistor R178 is connected to the inverting input of the amplifier U4. The other lead of the resistor R178 is coupled to a lead of the 100 picofarad capacitor C165. The other lead of the capacitor C165 is coupled to the cathode of a BB512 varactor diode D14. The anode of the diode D14 is coupled to a collector terminal of the NPN transistor Q16. The emitter terminal of the transistor Q16 is grounded. Transistor Q16 is turned on by placing the appropriate digital voltage signal on a BOOST0 lead which is coupled to the base terminal of the transistor Q16 through a 2 K ohm resistor R206. A variable reverse bias voltage is supplied on a CTRL10 line through a 100 K ohm resistor R174 connected to the junction of capacitor C165 and the cathode of varactor diode D14.

A second variable impedance comprises a 499 ohm resistor R184, an 82 picofarad capacitor C179, a BB512 varactor diode D21 and an NPN transistor Q22. One lead of the resistor R184 is coupled to the junction of resistor R178 and the capacitor C165. The other lead of the resistor R184 is coupled to a lead of the capacitor C179. The other lead of capacitor C179 is coupled to a cathode of varactor diode D21, while the anode of varactor diode D21 is coupled to the collector terminal of transistor Q22. The emitter terminal of transistor Q22 is grounded. Transistor Q22 is turned on by an appropriate digital logic signal supplied on a BOOST3 lead, that is connected through a 2 K ohm resistor R238 to the base terminal of the transistor Q22. A variable reverse bias voltage is supplied on a CTRL13 line through a 100 K ohm resistor R218 that is coupled to the junction of capacitor C179 and the cathode of varactor diode D21.

A third variable impedance comprises a 1.5 K ohm resistor R205, a 180 picofarad capacitor C189, a BB512 varactor diode D24 and an NPN transistor Q31. A lead of the resistor R205 is coupled to the junction of resistor R184 and capacitor C179. Another lead of resistor R205 is coupled to a lead of the capacitor C189. The other lead of capacitor C189 is coupled to the cathode of varactor diode D24, while the cathode of the varactor diode D24 is coupled to a collector terminal of transistor Q31. The emitter terminal of transistor Q31 is grounded. The transistor Q31 is turned on by supplying a digital logic signal on a BOOST5 line through a 2 K ohm resistor R246 that is coupled to a base terminal of the transistor Q31. A variable reverse bias voltage is supplied to the varactor diode D24 on an LF10 line through a 100 K ohm resistor R231 that is coupled to the junction of capacitor C189 and the anode of varactor diode D24.

For short cables, it is sometimes necessary to desensitize the amplifier U4 to the variable impedance as described above. Therefore, a 301 ohm resistor R157 is coupled between an inverting input of the amplifier U4 and a collector terminal of a transistor Q13. An emitter terminal of transistor Q13 is grounded. The transistor is turned on by a digital logic signal applied on a BOOST6 line through a 2 K ohm resistor R151 that is coupled to a base terminal of the transistor Q13.

The output of the amplifier U4 is coupled through a 49.9 ohm resistor R172 to a noninverting input of an operational amplifier U5. Again, the amplifier is connected in a noninverting configuration with a 301 ohm resistor R193 coupled between an output of the amplifier and an inverting input. Connected between the inverting input and ground is a 4.99 K ohm resistor R204. To compensate for

additional losses in the twisted wire cable, a plurality of variable impedances are also connected in the feedback path of the amplifier. A first variable impedance comprises a 10 ohm resistor R203, a 10 picofarad capacitor C186, a BB640 varactor diode D20 and an NPN transistor Q26. One lead of the resistor R203 is coupled to an inverting input of the amplifier U5. Another lead of the resistor R203 is coupled to a lead of the capacitor C186. The other lead of capacitor C186 is coupled to the cathode of the varactor diode D20, while the anode of diode D20 is coupled to a collector terminal of the transistor Q26. The emitter terminal of transistor Q26 is grounded. A variable reverse bias voltage is supplied on a CTRL11 lead through a 100 K ohm resistor R221 that is coupled to the junction of capacitor C186 and diode D20. The transistor Q26 is turned on by a digital logic signal supplied on a BOOST1 line through a 2 K ohm resistor R245 coupled to a base of the transistor Q26.

A second variable impedance comprises a 200 ohm resistor R212, a 33 picofarad capacitor C194, a BB640 varactor diode D27, and an NPN transistor Q30. One lead of the resistor R212 is coupled to the junction of resistor R203 and capacitor C186. The other lead of resistor R212 is coupled to a lead of the capacitor C194. The other lead of capacitor C194 is coupled to the cathode of diode D27, while the anode of diode D27 is coupled to a collector terminal of the transistor Q30. The emitter terminal of transistor Q30 is grounded. A variable reverse bias voltage is supplied to the diode D27 on a CTRL12 line through a 100 K ohm resistor R229, which is coupled to the junction of the capacitor C194 and diode D27. The transistor Q30 is turned on by a digital logic signal supplied on a BOOST2 line through a 2 K ohm resistor R249 that is coupled to a base terminal of the transistor Q30.

A third variable impedance comprises a 909 ohm resistor R217, a 180 picofarad capacitor C195, a BB512 varactor diode D30 and an NPN transistor Q34. One lead of the resistor R217 is coupled to the junction of resistor R212 and capacitor C194. The other lead of resistor R217 is coupled to a lead of the capacitor C195. The other lead of capacitor C195 is coupled to the cathode of varactor diode D30, while the anode of diode D30 is coupled to a collector terminal of transistor Q34. The emitter terminal of transistor Q34 is grounded. A variable reverse bias voltage is supplied on an LF11 line through a 100 K ohm resistor R230 that is coupled to the junction of capacitor C195 and diode D30. The transistor Q34 is turned on by a digital logic signal applied on a BOOST4 lead through a 2 K ohm resistor R250 coupled to a base terminal of the transistor Q34.

The output of the amplifier U5 is coupled through a 49.9 ohm resistor R171 to a buffer amplifier (not shown). The output of the buffer amplifier is sent to the appropriate input of a color monitor.

The following table defines the reverse bias DC voltages that are applied to the varactor diodes in order to compensate for various lengths of twisted wire cables.

LENGTH OF CABLE	CTRL10	CTRL11	CTRL12	CTRL13	LF10	LF11	DC
25	X	FF	X	X	5C	X	40
50	X	FF	X	X	X	69	40
100	C5	9E	X	X	2E	69	40
150	X	FF	X	5C	48	X	50
200	X	FF	X	6A	48	X	50
250	X	01	X	5C	28	5C	50
300	FF	X	7	69	9F	42	55
350	C0	X	7	52	80	36	55
400	A2	X	7	40	40	30	55
450	60	FF	7	30	25	25	55
500	45	7F	7	27	15	21	60
550	45	5C	7	27	0D	0A	60
600	21	5C	7	27	0D	05	60

The following table describes the logic used to enable the transistors to turn on the varactor diodes in each of the variable impedances to boost the gain of the amplifiers.

LENGTH OF CABLE	BOOST0	BOOST1	BOOST2	BOOST3	BOOST4	BOOST5	BOOST6
25	0	1	0	0	0	1	1
50	0	1	0	0	1	0	1
100	0	1	0	0	0	1	1
150	0	1	0	1	0	1	0
200	0	1	0	1	0	0	0
250	0	1	0	1	1	1	0
300	1	0	1	1	1	1	0
350	1	0	1	1	1	1	0
400	1	0	1	1	1	1	0
450	1	1	1	1	1	1	1
500	1	1	1	1	1	1	1
550	1	1	1	1	1	1	1
600	1	1	1	1	1	1	1

A 0 in the table indicates a logic low signal, while a 1 indicates a logic high signal, and an x indicates a don't care condition. The logic signals are supplied by a latching circuit that is controlled by the microprocessor 170, shown in FIGURE 2.

As will be appreciated, in order to compensate the three colors provided in the video signal, two additional circuits of the type shown in FIGURE 4 are required for the other two video colors.

As can be seen from the above description, the present invention allows high-frequency signals such as video signals to be transmitted on twisted wire cables up to 600 feet in length. However, those skilled in the art will recognize that additional lengths could be accommodated using the same techniques. Because the loss curve of the twisted wire cables does not exhibit a simple slope with respect to frequency, numerous compensation stages must be provided to create a piecewise linear fit. Using the compensation system of the present invention, response curves that are flat to within ± 1 dB up to 100 MHz or more, can be obtained using Category 5 cable up to 600 feet in length.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention. It is therefore intended that the scope of the claims be determined from the following claims and equivalents thereto.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A system for compensating high-frequency signal losses in a twisted wire cable, comprising:

a differential receiver that receives a differential signal on a twisted wire cable;

one or more equalizing networks that receive a signal from an output of the differential receiver, the equalizing networks including a feedback controller amplifier having a variable impedance disposed in a feedback path, the variable impedance including a varactor diode having a capacitance that varies in accordance with a reverse bias voltage applied to the diode, and a circuit that applies a variable reverse bias voltage to the varactor diode in accordance with a length of the twisted wire cable to be compensated.

2. The system of Claim 1, wherein the feedback controlled amplifier comprises an operational amplifier having an inverting and a non-inverting input, and wherein the variable impedance comprises a fixed capacitor disposed between the non-inverting input and the varactor diode.

3. The system of Claim 2, wherein the variable impedance comprises a fixed resistor disposed between the non-inverting input of the operational amplifier and the fixed capacitor.

4. The system of Claim 1, wherein the circuit that applies a variable reverse bias voltage to the varactor diode comprises a digital-to-analog converter.

5. The system of Claim 4, wherein the circuit that applies a variable reverse bias voltage to the varactor diode further comprises a microprocessor that supplies a binary value to the digital-to-analog converter, wherein the binary value is selected in accordance with the length of the twisted wire cable to be compensated.

6. The system of Claim 5, wherein the circuit that applies a variable reverse bias voltage to the varactor diode further comprises a buffer amplifier disposed between the digital-to-analog converter and the varactor diode

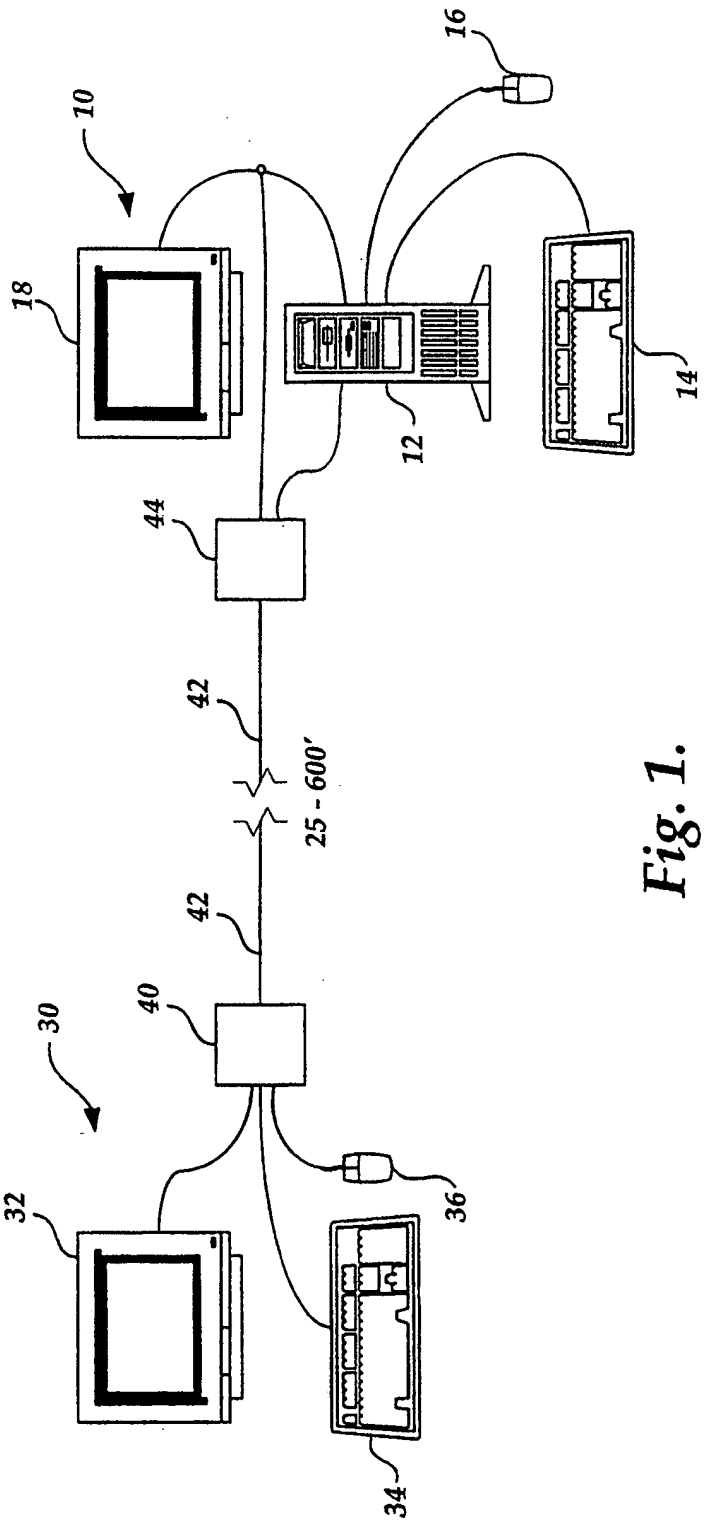

Fig. 1.

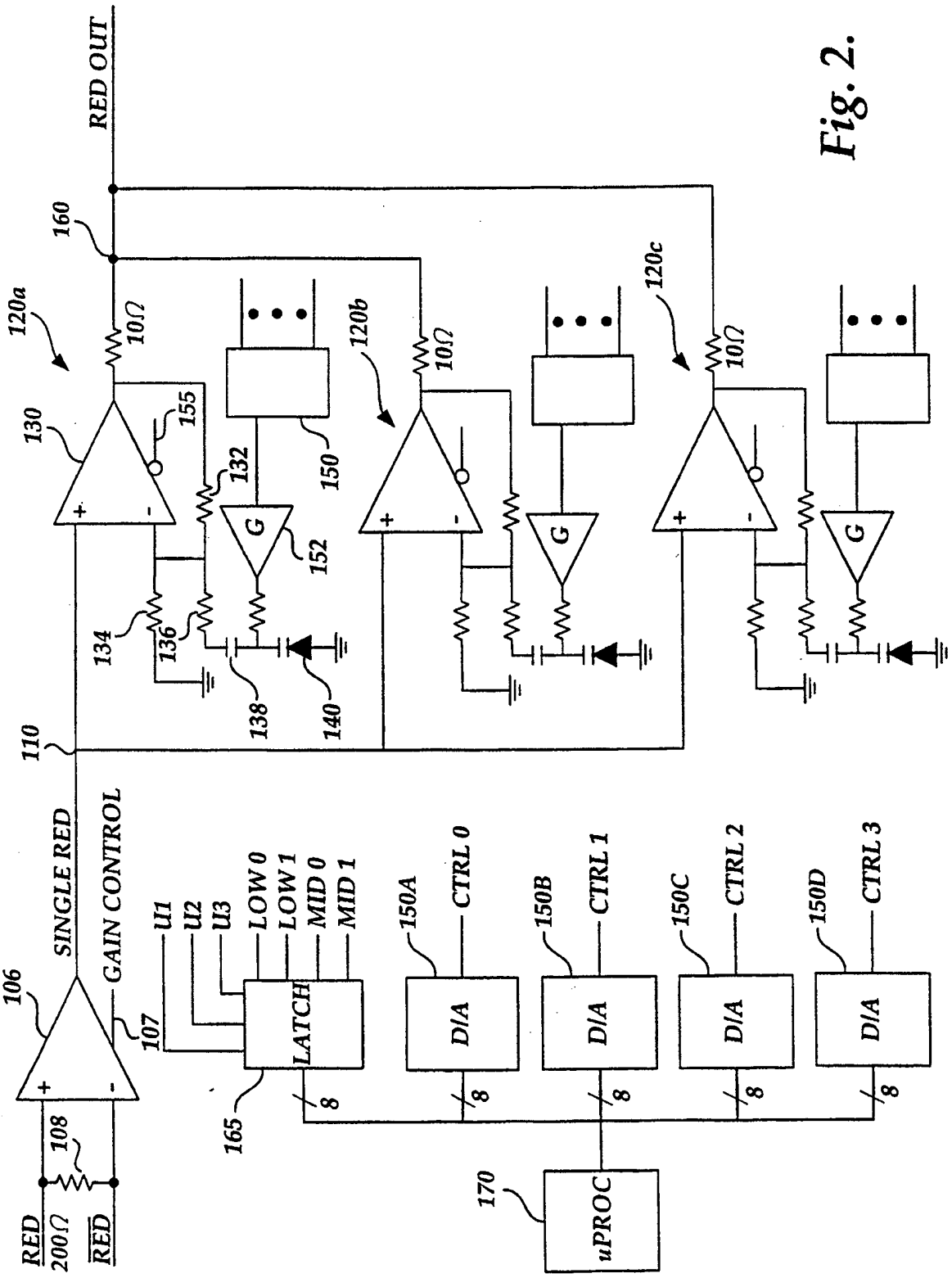
RED OUT
160
120a
120b
120c
10Ω
130
155
132
150
152
G
134
136
138
140
110
SINGLE RED
GAIN CONTROL
106
107
108
RED
200Ω
RED
U1
U2
U3
LOW 0
LOW 1
MID 0
MID 1
LATCH
165
8
150A
CTRL 0
150B
CTRL 1
150C
CTRL 2
150D
CTRL 3
D/A
170
uPROC

Fig. 2.

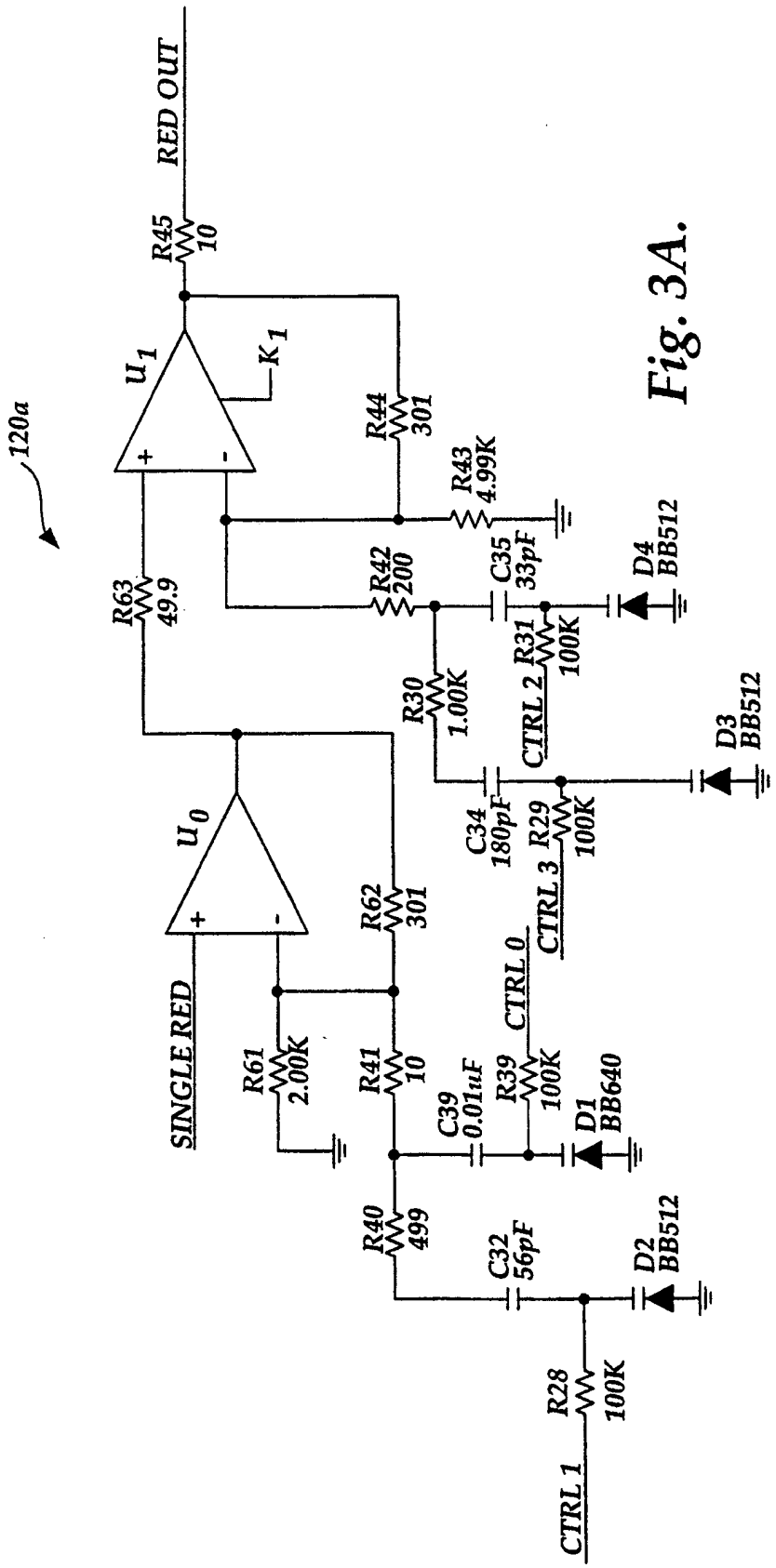
120a
RED OUT
R45 10
U1
K1
R44 301
R43 4.99K
D4 BB512
C35 33pF
R42 200
R63 49.9
R31 100K
CTRL 2
R30 1.00K
D3 BB512
C34 180pF
R29 100K
CTRL 3
U0
R62 301
CTRL 0
SINGLE RED
R61 2.00K
R41 10
C39 0.01uF
R39 100K
D1 BB640
R40 499
C32 56pF
D2 BB512
R28 100K
CTRL 1

Fig. 3A.

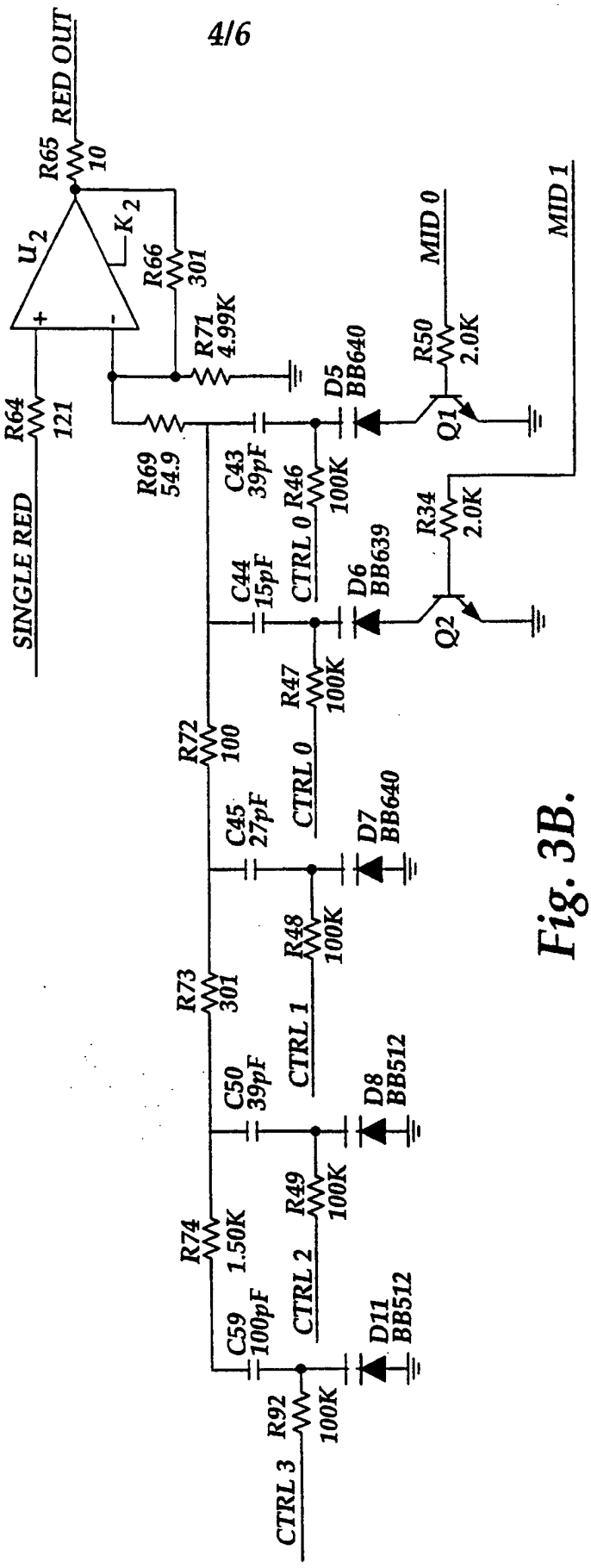
RED OUT
R65
10
U2
K2
R66
301
R71
4.99K
MID 0
R50
2.0K
D5
BB640
Q1
MID 1
R64
121
R69
54.9
C43
39pF
R46
100K
CTRL 0
R34
2.0K
SINGLE RED
C44
15pF
D6
BB639
Q2
R47
100K
R72
100
C45
27pF
CTRL 0
D7
BB640
R48
100K
R73
301
CTRL 1
C50
39pF
D8
BB512
R49
100K
R74
1.50K
CTRL 2
C59
100pF
D11
BB512
R92
100K
CTRL 3

Fig. 3B.

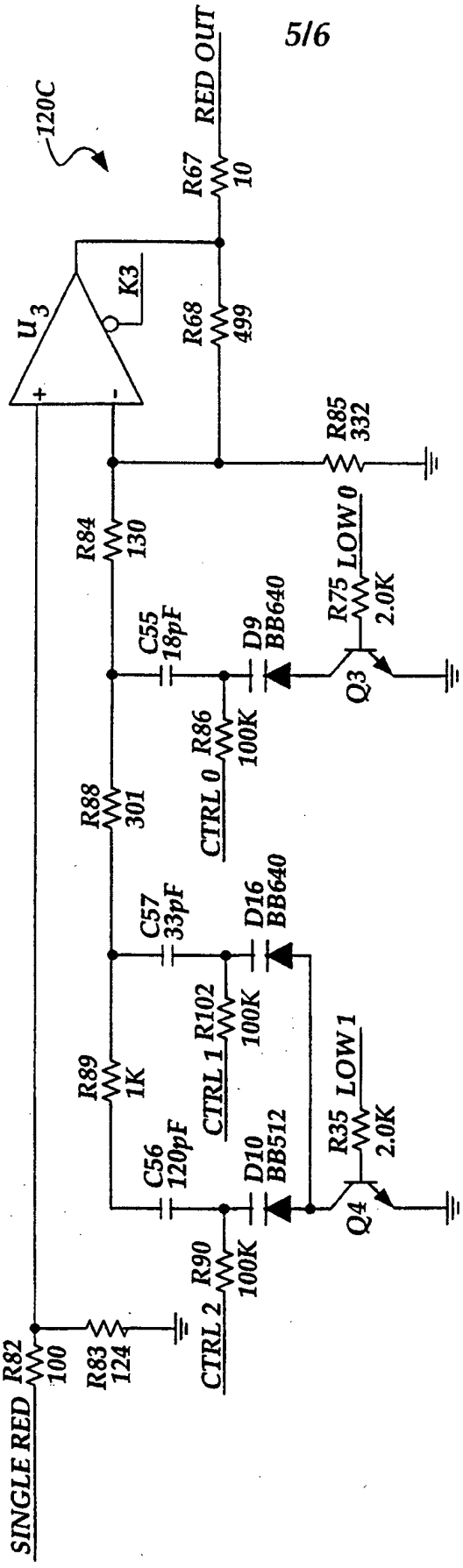
120C
RED OUT
R67
10
K3
U3
R68
499
R85
332
R84
130
C55
18pF
D9
BB640
R75
LOW 0
2.0K
Q3
R86
100K
CTRL 0
R88
301
C57
33pF
D16
BB640
R102
100K
CTRL 1
R89
1K
C56
120pF
D10
BB512
R35
LOW 1
2.0K
Q4
R90
100K
CTRL 2
R82
100
R83
124
SINGLE RED

Fig. 3C.

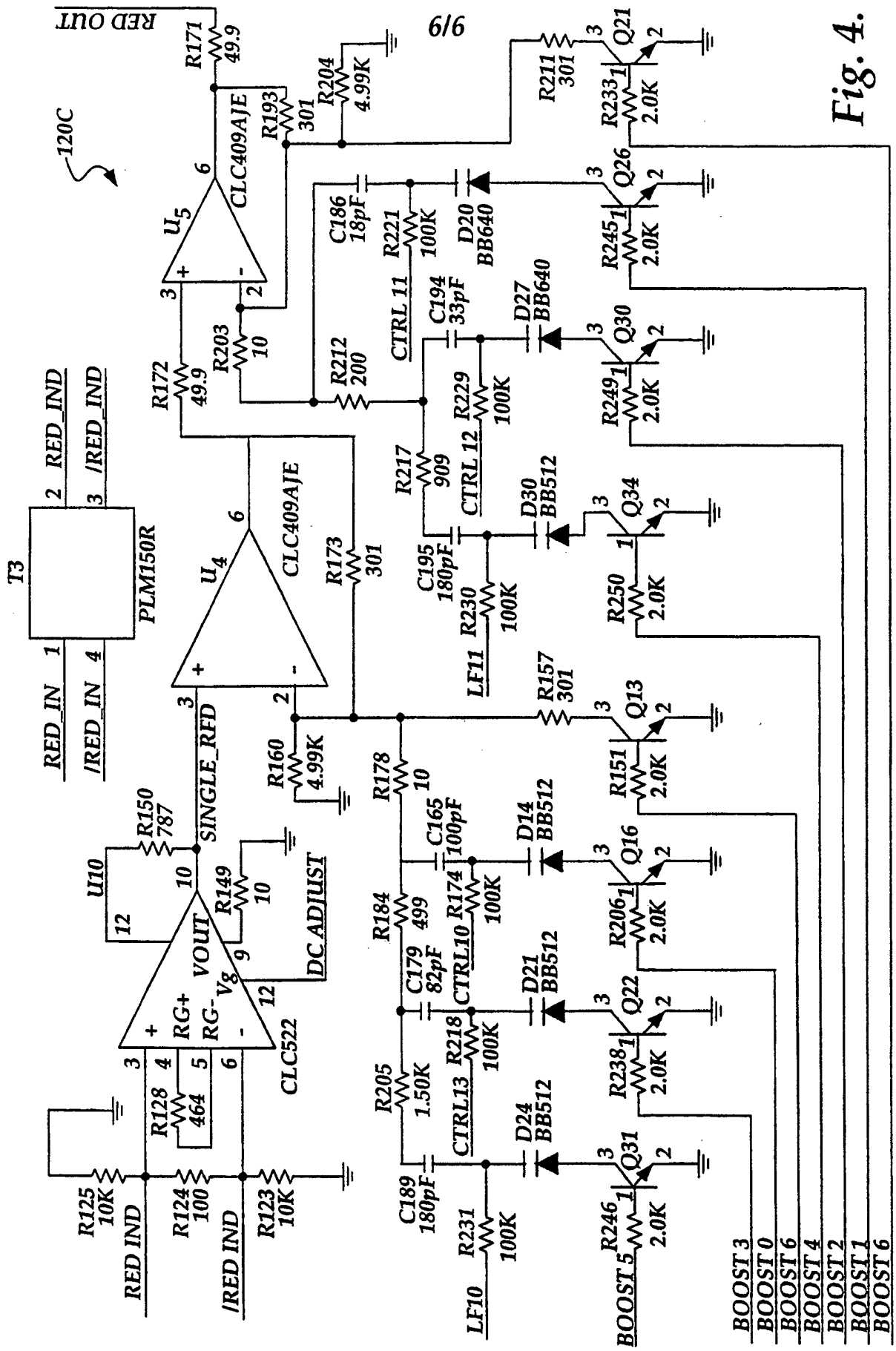
6/6
120C
RED OUT
R171 49.9
U5 CLC409AJE
R193 301
R204 4.99K
R211 301
Q21
R233 2.0K
Q26
R245 2.0K
C186 18pF
R221 100K
D20 BB640
CTRL 11
C194 33pF
D27 BB640
Q30
R249 2.0K
R203 10
R212 200
R172 49.9
R229 100K
R217 909
CTRL 12
D30 BB512
Q34
R250 2.0K
C195 180pF
R230 100K
LF11
R157 301
Q13
R151 2.0K
T3
PLM150R
RED_IN
/RED_IN
RED_IND
/RED_IND
U4 CLC409AJE
R173 301
R160 4.99K
R178 10
D14 BB512
Q16
R206 2.0K
C165 100pF
R174 100K
R184 499
C179 82pF
CTRL10
D21 BB512
Q22
R238 2.0K
R218 100K
R205 1.50K
CTRL13
D24 BB512
Q31
R246 2.0K
C189 180pF
R231 100K
LF10
BOOST 5
BOOST 3
BOOST 0
BOOST 6
BOOST 4
BOOST 2
BOOST 1
BOOST 6
U10
R150 787
SINGLE_RFD
R149 10
DC ADJUST
VOUT
Vg
RG+
RG-
CLC522
R128 464
R125 10K
R124 100
R123 10K
RED IND
/RED IND

Fig. 4.

VERSION*

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(74) Agent: TULLETT, Rodney, C.; Christensen O'Connor Johnson & Kindness, Suite 2800, 1420 Fifth Avenue, Seattle, WA 98101 (US).

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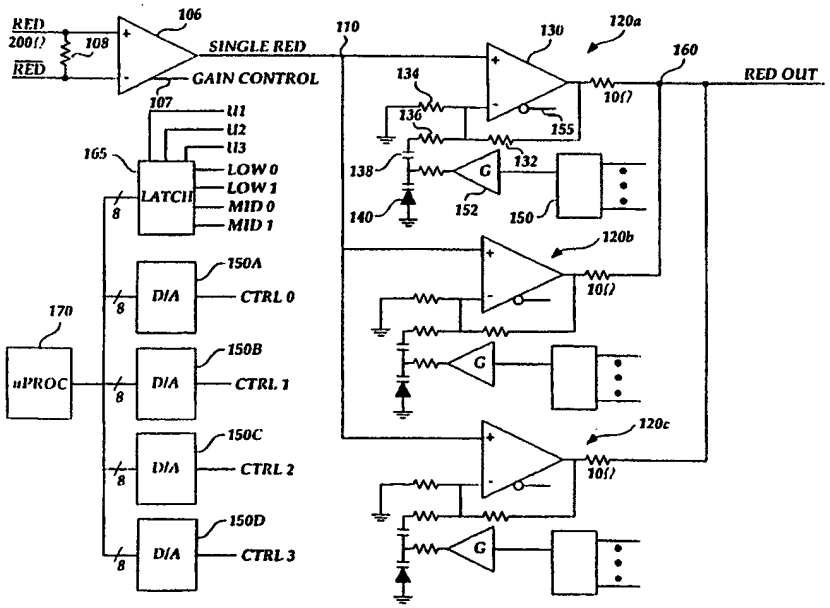

(57) Abstract

An equalization system for compensating the attenuation of high-frequency signals in a twisted wire cable. An equalizing circuit comprises a number of operational amplifiers with a variable impedance connected in a feedback path. The variable impedance comprises a varactor diode whose capacitance changes with the magnitude of a reverse bias voltage. The reverse bias voltage is controlled using a digital-to-analog converter and a gain amplifier to increase the gain of the operational amplifiers at high frequencies. A microprocessor selects the appropriate reverse bias voltages depending on the length of the twisted wire cable to be compensated.

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INTERNATIONAL SEARCH REPORT

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According to International Patent Classification (IPC) or to both national classification and IPC

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Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 310 237 A (BABCOCK & WILCOX CO) 5 April 1989 see abstract see column 1, line 13 - line 34 see column 6, line 42 - column 7, line 18; figures 6,8	1-6
A	US 4 888 560 A (OGURA YOICHI) 19 December 1989 see column 1, line 38 - line 61; figure 11 see column 9, line 23 - line 45	1-6

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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De Iulis, M

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